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User Manual

PMC-Serial-RTN5

Quad UART - Dual Synchronous Serial Data Interface PMC Module

Manual Revision B
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PMC-Serial
Quad UART - Dual Synchronous Serial Data Interface PMC Module

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Product Description

PMC-Serial is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-Serial is capable of providing multiple serial protocols both synchronous and asynchronous with a wide range of baud rates. The RTN5 interface has two UART [A,B] channels set-up with RS-422 and two channels with RS-232 [C,D]. The SCC is configured with RS-232 IO. Two enhanced hysteresis MIL STD 188-114A receivers, and two open drain active low output drivers are also provided.

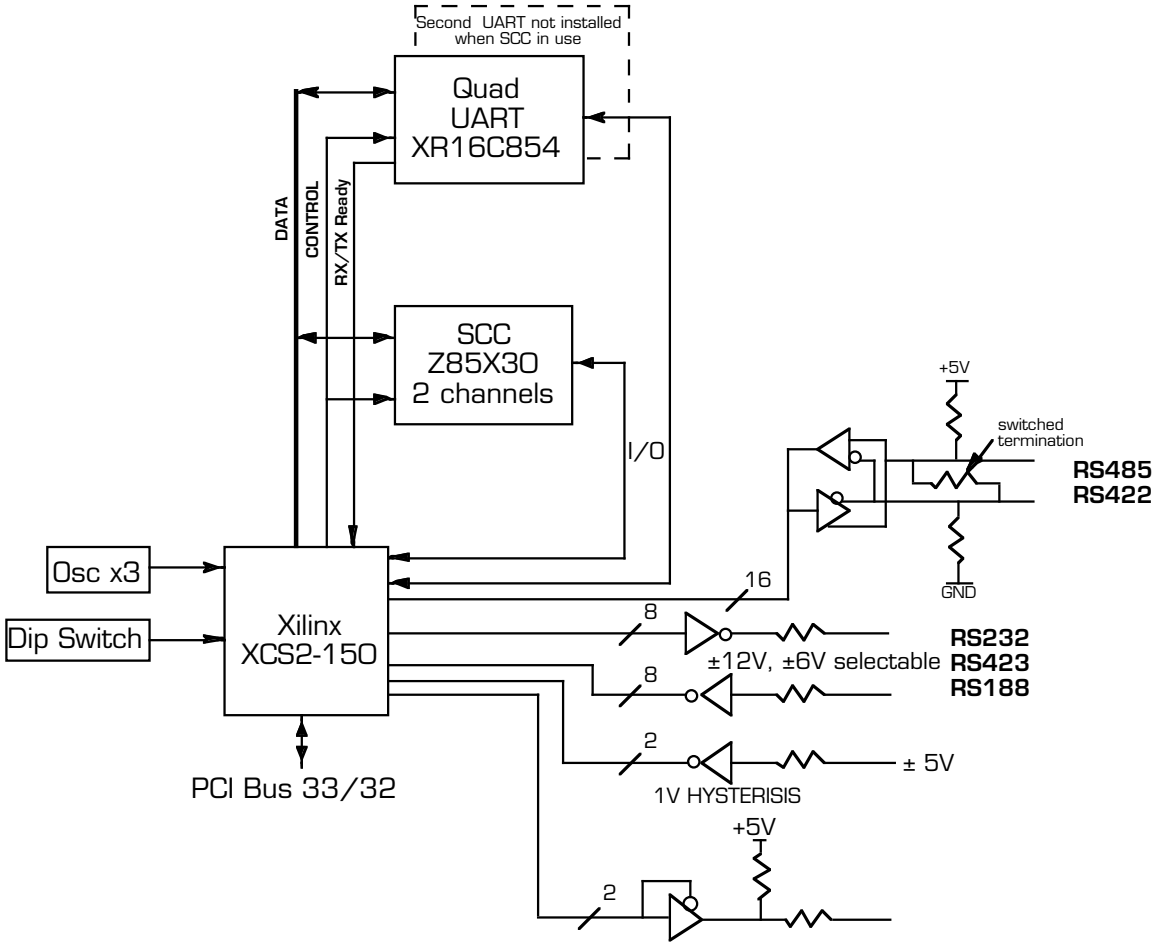

FIGURE 1 PMC-SERIAL BLOCK DIAGRAM

Other configurations are built into the board layout, including a second quad UART replacing the SSC, and RS-485 I/O. Different oscillators can be installed, or other modifications can be made to accommodate your particular requirements. The new variation will be offered as a "standard" special order product. Please see our web page for current products offered and contact Dynamic Engineering with your custom application.

An EXAR XR16C854 implements the UART interface. This quad UART device is compatible with the industry standard 16550 UART, and is equipped with 128 byte FIFOs, independent Tx and Rx FIFO counters, automatic hardware/software flow control, and many other enhanced features. The Xilinx design supports the UARTs with a pre-read function and internal memory to allow for pipelined access with lower latency than would otherwise be possible. In addition the character based UART data can be interfaced with wider words. Please see the programming section for more information.

Three oscillators are installed on the board: 12.288 MHz, 18.432 MHz, and 24.000 MHz. These are connected to the Xilinx to allow software selection of the clock source for the serial chips.

The synchronous interface uses a Zilog Enhanced Serial Communication Controller, the Z85230. This dual channel, multi-protocol device can implement various bit-oriented and byte-oriented synchronous protocols such as HDLC and IBM BiSync and handles asynchronous formats as well.

The PMC-Serial also has a wide range of IO drivers and receivers to interface with. The SCC and UART IO are tied to the Xilinx and then back to the IO to allow for programmable options and ease of customerization.

Up to a total of 24 IO can be installed. The RS-232 and RS-485 can be configured in groups of 4. 4 RS-232 TX, 4 RS-232 RX swapped with 4 RS-485. There are 24 differential RS422/485 transceiver locations that can be configured as either receivers or transmitters, 24 single-ended RS188/232/423 drivers operating at selectable voltage levels, and 24 single-ended receivers capable of up to +/- 25V input range.

There are two enhanced hysteresis (~1.5V) RS423 receivers for handling noisy input signals and two open drain outputs that sink up to 65 mA.

The differential input signals are selectively terminated with switched 100Ω terminations. When the channels are set to RS-485 the analog switch(s) and termination resistor(s) are installed to allow for programmable termination. All single ended lines have series 22Ω resistors for circuit protection.
All configuration registers internal to the Xilinx support read and write operations for software convenience. All addresses are long word aligned including the UART and SCC internal registers even though they only have
and termination resistor(s) are installed to allow for programmable termination. All single ended lines have series 22Ω resistors for circuit protection.

All configuration registers internal to the Xilinx support read and write operations for software convenience. All addresses are long word aligned including the UART and SCC internal registers even though they only have byte-wide registers. Please see the XR16C854 and Z85230 data sheets and user's manuals for more information on register access and functions.

The PMC-Serial conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

PMC-Serial uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors [height] to mate with the PMC-Serial, please let us know. We may be able to do a special build with a different height connector to compensate.

Interrupts are supported by the PMC-Serial. Each of the four UARTs and the SCC has a maskable input to the interrupt generation logic in the Xilinx. There is also a master interrupt enable that must be set to gate the interrupt onto the PCI bus. The interrupt status is still available in a status register even when the master interrupt enable is off. This facilitates polled operation of interrupt conditions. The individual interrupt conditions are specified in the internal registers of the UART and SCC. Please see the XR16C854 and Z85230 documentation for more information on interrupt conditions and configuration.

Theory of Operation

The PMC-Serial is designed for transferring data from one point to another with a variety of serial protocols.

The PMC-Serial features a Xilinx FPGA, which contains the general control and status registers as well as the interface to the quad UART, SCC, and IO drivers and receivers. Many additional control and status registers reside in the UART and SCC, which are accessed through the Xilinx interface.

The PMC-Serial is a part of the PMC family of modular I/O products, which meet the PMC and CMC draft Standards. In standard configuration, the PMC-Serial is a Type 2 mechanical with only passive low profile components on the back of the board and one slot wide, with 10 mm inter-board height.

A logic block within the Xilinx implements the PCI interface to the host CPU. The PMC-Serial design requires one wait state for read or write cycles to addresses other than the SCC or UART which require from three for a simple write operation to nine for the SCC interrupt acknowledge/vector read cycle. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus, and to convert the "terminate with data" state into the TRDY signal.

The quad UART and dual Serial Communication Controller can handle multiple asynchronous and synchronous protocols and the IO drivers and receivers support a range of electrical interface standards.

The clock input for the UART can be driven by any of the three oscillators or the PCI clock. In addition, the UART C channel has its own clock input, which can be selected independently of the clock for the other three channels. The clock input for the SCC can be driven by the 12.288 MHz or the 18.432 MHz oscillator.

Each of the four UART channels and the two synchronous serial channels has its own on-board 16-bit baud rate generator to supply a wide range of clock reference frequencies. The SCC can also operate from external clock sources with separate Rx clock input and Tx clock input/output pins for each channel.

Even though the UART data bus is only eight bits wide, 16-bit and 32-bit accesses for Tx and Rx data can be enabled on a per-channel basis. On a write cycle the data is latched and the bus cycle will terminate immediately. The data is then written into the UART Tx FIFO as a background process. During this time the bus is free for accesses other than the UART or SCC, which will not be available until the writes are complete. The 16-bit and 32-bit read functions are similar, but the bus is not released until the UART reads have completed and the data is enabled onto the bus.

If the background pre-read function is enabled, the RXRDYA-D lines are

used to determine when data is available to be read from the Rx FIFO for the respective channel. An eight-byte circular buffer is provided for each channel and when data is available, it is automatically read and stored in this buffer. If more than one channel needs to be serviced simultaneously they will be read in a round-robin pattern as long as data is available and the storage is not full. The data in these buffers is read just like a normal data read, but only one wait state is required for the access. Either one, two, or four bytes will be read in a cycle depending on whether 16-bit or 32-bit data reads are enabled.

It should be noted that these two features are intended for data accesses only, since all the internal registers in the UART are eight bits wide. Therefore the special accesses only occur when the lower address bits are all zero, however, the UART has shadow registers at the same address as the data ports that are used for configuration. These shadow registers are enabled by writing certain bits in other registers e.g. the lower byte of the baud-rate setting is enabled at this address when the Line Control Register bit 7 is set to '1'. Therefore it is important that these special registers are disabled before the enhanced data access features are enabled. Please refer to figure 2 and the XR16C854 data sheet for information on enabling and disabling these registers.

If data is requested from the pre-read data store when there is not sufficient data stored to satisfy the request, the bus acknowledge will be held off until the data is present causing the PCI bus to hang. To avoid this, a user programmable watchdog timer is supplied to complete the bus cycle and issue an interrupt if the timer expires. The timer count is programmed by writing a value to the PMC_SER_TIMEOUT register. If this value is zero, the counter never expires; otherwise the value is the number of PCI clocks before the bus cycle is aborted. The data read when the timeout occurs comes from the PMC_SER_TIMEOUT_DATA register and can be set to any value desired.
When RS-422/485 transceivers are utilized with the SCC, their direction pre-determined in full-duplex mode, and in half-duplex mode the direction of the IO is controlled by the PMC_SER_DIR register. In either mode the switched terminations are controlled by the PMC_SER_TERM register. See the bit definitions in the PMC_SER_BASE control register for the various options for IO connections to the SCC signals.

When RS-232 IO is used with the SCC, the direction of the bits is fixed, the direction and termination registers are not used, and half duplex operation is not possible.

Please refer to the XR16C854 and Z85230 documentation for more information on the operation and capabilities of these devices.

Address Map

REGISTER	OFFSET	FUNCTION	TYPE
PMC_SER_BASE	0X0000	base control	read/write
PMC_SER_SW_IN	0X0004	read user switch	read
PMC_SER_INTSTAT	0X0008	interrupt status read	read
PMC_SER_IRUPT_CLR	0X0008	interrupt latch clear	write
PMC_SER_TERM	0X0010	termination control	read/write
PMC_SER_DIR	0X0014	direction control	read/write
PMC_SER_DATA_SRC_422	0X0018	I/O data source selection	read/write
PMC_SER_DATA_422	0X001C	alternate I/O data source	read/write
PMC_SER_DATA_422RDBK	0X0020	RS-422 input data	read
PMC_SER_DATA_SRC_232	0X0024	232/TTL data source selection	read/write
PMC_SER_DATA_232	0X0028	alternate 232/TTL data source	read/write
PMC_SER_DATA_232RDBK	0X002C	RS-232 / AUX input data	read/write
PMC_SER_TIMEOUT	0X0038	Timeout count and enable	read/write
PMC_SER_TIMEOUT_DATA	0X003C	Timeout bus data	read/write
PMC_SER_CNTLA	0X0040	UART A control	read/write
PMC_SER_CNTLB	0X0044	UART B control	read/write
PMC_SER_CNTLC	0X0048	UART C control	read/write
PMC_SER_CNTLD	0X004C	UART D control	read/write
PMC_SER_SCC_A_CNTL	0X0088	SCC channel A control	read/write
PMC_SER_SCC_A_DATA	0X008C	SCC channel A data	read/write
PMC_SER_SCC_B_CNTL	0X0090	SCC channel B control	read/write
PMC_SER_SCC_B_DATA	0X0094	SCC channel B data	read/write
PMC_SER_SCC_INTACK	0X00C0	SCC interrupt acknowledge	read/write
PMC_SER_QUART_A	0X0100	UART A base offset	read/write
PMC_SER_QUART_B	0X0120	UART B base offset	read/write
PMC_SER_QUART_C	0X0140	UART C base offset	read/write
PMC_SER_QUART_D	0X0160	UART D base offset	read/write

FIGURE 2 PMC-SERIAL ADDRESS MAP

Each UART channel has a number of registers associated with it. These register offsets and their general functions are given in figure 3. For details of the bits and functions of each register consult the documentation for the XR16C854.

The SCC also has a number of internal registers that are accessed in a two-step process. First the register number is written to the control address for the respective channel. Then an additional read or write to the same control address is performed. This causes the data to be read from or written to the desired register. At the end of this process the register pointer is reset so that the next access is again to/from the base control register. For a more complete description of this process, as well as details of registers and their functions, see the user's manual for the Z85230.

The address map provided is for the local decoding performed within the PMC-Serial. The addresses are all offsets from a base address. The carrier board that the PMC is installed into provides the base address.

The VendorId = Ox10EE. The CardId = Ox001F. Current revision = Ox01

REGISTER	OFFSET	FUNCTION
UART_DATA	0X00	UART read/write data
UART_IEN	0X04	UART write interrupt enable
UART_ISTAT	0X08	UART read interrupt status
UART_FCNTL	0X08	UART write FIFO control
UART_LCNTL	0X0C	UART write line control
UART_MCNTL	0X10	UART write modem control
UART_LSTAT	0X14	UART read line status
UART_MSTAT	0X18	UART read modem status
UART_SPAD	0X1C	UART read/write scratchpad
UART baud rate register defines (enabled when *LCNTL bit-7 = 1)		
UART_DLL	0X00	UART read/write LSB divisor
UART_DLM	0X04	UART read/write MSB divisor
UART enhanced register offsets (enabled when *LCNTL = 0xBF)		
UART_FTC	0X00	UART FIFO read count/write trigger level
UART_FEAT	0X04	UART write feature control
UART_ENF	0X08	UART read/write enhanced features
UART_XON1	0X10	UART read/write Xon-1 word
UART_XON2	0X14	UART read/write Xon-2 word
UART_XOFF1	0X18	UART read/write Xoff-1 word
PMC_UART_XOFF2	0X1C	UART read/write Xoff-2 word
UART EMS registers (enabled when feature control bit-6 = 1)		
PMC_UART_EMS	0X1C	UART write enhanced mode select

FIGURE 3 PMC-SERIAL UART ADDRESS MAP

Programming

Programming the PMC-Serial requires only the ability to read and write data from the host. The PMC Carrier board determines the base address, which refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC-Serial "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware. The PMC-Serial VendorId = 0x10EE. The CardId = 0x001F. Current revision = 0x01

The interrupt service routine should be loaded, the interrupt mask set, and the desired interrupt conditions set up in the UART and SCC. Each of the four UART channels and the SCC has a separate interrupt enable in the Xilinx as well as various interrupt conditions that can be set up in their internal registers.

Refer to the Theory of Operation section above, the Register section below, and the XR16C854 and Z85230 documentation for more information regarding the register functions and definitions.

Register Definitions

PMC_SER_BASE

[0X00] PMC-SERIAL Control Register read/write

CONTROL BASE

DATA BIT	DESCRIPTION
31	not invert SCC RTS A
30	SCC B half duplex DCD select
29	SCC B half duplex RTxClock select
28	SCC B Sync | DTR/Req select
27	SCC B W/Req | TRxClock select
26	SCC B Sync/DCD select
25	SCC B external clock select
24	SCC B TRxClock input select
23	SCC B Sync input select
22	SCC B half duplex select
21	SCC A half duplex DCD select
20	SCC A half duplex RTxClock select
19	master interrupt enable
18	force interrupt
17	SCC A Sync | DTR/Req select
16	SCC A W/Req | TRxClock select
15	SCC A Sync | DCD select
14	SCC A external clock select
13	SCC A TRxClock input select
12	SCC A Sync input select
11	SCC A half duplex select
10	SCC clock select
9	SCC interrupt enable
8	SCC reset
7	UART FIFO status read enable
6	timeout interrupt enable
5,4	UART C clock select
3,2	UART clock select
1	UART pre-divide disable
0	UART reset

FIGURE 4 PMC-SERIAL BASE CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

UART reset causes a hardware reset of the UART. In order to accomplish this, set this bit high and then low. All registers and modes in the UART will revert to the reset state.
UART pre-divide disable: When this bit is set to a one during a UART reset the divide by four prescaler in UART channels A – D is disabled, if the bit is a zero during reset the input clock is divided by four before being routed to the baud rate generator. This function can be overridden by bit 7 in the MCR register for each channel.

UART clock select: These two bits select the input clock for UART channels A, B, and D according to the following table.

00	18.432 MHz
01	24.000 MHz
10	12.288 MHz
11	PCI clock

UART C clock select: These two bits select the input clock for UART

channel C with the same selections as above.

Timeout Interrupt Enable: When this bit is set to a one the timeout interrupt is enabled, a zero disables the interrupt. This allows the bus watchdog timer to cause an interrupt if a bus cycle does not terminate properly. This is intended for the pre-read function of the UART receive data. If insufficient data is available to satisfy a read request when the pre-read function is enabled, the state machine will wait for data to be available before completing the request rather than returning erroneous data. If no more data is received, the cycle will hang. The timeout interrupt notifies the host that such a condition exists.

UART FIFO status read enable: When this bit is set to a one, any read from the UART returns the status of the four Tx and four Rx FIFOs. Data bits 0-3 indicate the state of TxA-TxD respectively. A one indicates that the FIFO is ready to accept data, a zero indicates that the FIFO input is not available. Bits 4-7 indicate the state of RxA-RxD respectively. A one indicates that no data is available to be read, a zero indicates that there is data in the FIFO to be read.

SCC reset: causes a hardware reset of the SCC. The process is the same as the UART.

SCC interrupt enable: When this bit is set to a one, the SCC interrupt is enabled in the Xilinx, interrupt conditions must still be enabled in the SCC internal registers for the interrupt to function properly. When this bit is a zero the SCC interrupt is disabled.
SCC clock select: When this bit is set to a one the 18.432 MHz oscillator is routed to the SCC clock input. When this bit is a zero the 12.288 MHz oscillator is used to drive the SCC clock input.

SCC A/B half duplex select: When this bit is set to a one the half duplex IO mode is selected for the corresponding channel. When this bit is a zero, full duplex mode is selected. In half duplex mode, the direction control register determines whether an IO line functions as an input or an output. In full duplex mode the IO directions are fixed. In the –RTN5 design, RS-232 drivers and receivers with fixed directions are used for the SCC signals, therefore it is not possible to implement a traditional half duplex mode. However, this bit does affect which IO lines are connected to the various SCC signals. See the table at the end of this section for details of these connections.

SCC A/B Sync input select: When this bit is set to a one the bi-directional pin Sync on the corresponding channel is driven from the Xilinx. When this bit is a zero the Xilinx receives the signal from the Sync pin. The SCC pin direction must be configured independently with the SCC internal registers.

SCC A/B TRxClock input select: When this bit is set to a one the bi-directional pin TRxClock on the corresponding channel is driven from the Xilinx. When this bit is a zero the Xilinx receives the signal from the TRxClock pin. The SCC pin direction must be configured independently with the SCC internal registers.

SCC A/B external clock select (trc*insel): When this bit is set to a one in full duplex mode TRxClock is driven by IO7 for channel A or IO15 for channel B. If this bit is a zero RTxClock is used for the external clock input. In half duplex mode this bit has no effect.

SCC A/B Sync | DCD select (syc*insel): When this bit is set to a one in full duplex mode Sync is driven by IO5 for channel A or IO13 for channel B. If this bit is a zero DCD is driven by these inputs. In half duplex mode this bit has no effect.

SCC A W/Req | TRxClock select (wrq*outsel): When this bit is set to a one in full duplex mode W/Req drives IO6 for channel A or IO14 for channel B. If this bit is a zero TRxClock drives these outputs. In half duplex mode this bit has no effect.

SCC A Sync | DTR/Req select (syc*outsel): When this bit is set to a one in full duplex mode Sync drives IO4 for channel A or IO12 for channel B. If this bit is a zero DTR/Req drives these outputs. In half duplex mode this bit has no effect.

SCC A/B half duplex RTxClock select (rtc*hfsel): When this bit is set to a one in half duplex mode RTxClock is driven by IO2 for channel A or IO10 for channel B. If this bit is a zero RTxClock is driven by IO6 for channel A or IO14 for channel B. In full duplex mode this bit has no effect.

SCC A/B half duplex DCD select (dcd*hfsel): When this bit is set to a one in half duplex mode DCD is driven by IO0 for channel A or IO8 for channel B. If this bit is a zero DCD is driven by IO5 for channel A or IO13 for channel B. In full duplex mode this bit has no effect.

Force interrupt: When this bit is set to a one a system interrupt will occur provided the master interrupt enable is set. This is useful to stimulate interrupt acknowledge routines for development.

Master interrupt enable: When this bit is set to a one all enabled interrupts will be gated through to the PCI host. When this bit is a zero the interrupts can be used for status without interrupting the host.

Not Invert SCC RTS A: When set to '1' the SCC RTS signal for channel A operates in "normal mode". When set to '0' the RTS signal is inverted. Only affects the channel A RTS signal for the SCC. The default is to the inverted state.

Signal	Half Duplex Mode	Full Duplex Mode
STXA	pin 38	pin 4 and pin 38
SRXA	pin 36	pin 36
STRxClkA(input)	pin 41	pin 41 when trcainsel = 1 else auxin0
STRxClkA(output)	pin 43	pin 9 when wrqaoutsel = 0
SRTxClkA	pin 3 when rtcahfsel = 1 else pin 7	pin 41 when trcainsel = 0 else gnd
SSyncA(input)	pin 6	pin 40 when sycainsel = 1 else vcc
SSyncA(output)	auxout0 and pin 8	auxout0 and pin 8 when sycaoutsel = 1
SWrReqA	pin 9	pin 5 when wrqaoutsel = 0 else pin 9
SDtrReqA	pin 4 and pin 42	pin 42 and pin 8 when sycaoutsel = 0
SRTSA	pin 39	pin 5 and pin 39
SCTSA	pin 37	pin 37
SDCDA	pin 2 when dcdahfsel = 1 else pin 40	pin 40 when sycainsel = 0 else gnd
STXB	pin 47	pin 13 and pin 47
SRXB	pin 45	pin 45
STRxClkB(input)	pin 50	pin 50 when trcbinsel = 1 else auxin1
STRxClkB(output)	pin 52	pin 18 when wrqboutsel = 0
SRTxClkB	pin 12 when rtcbhfsel = 1 else pin 16	pin 50 when trcbinsel = 0 else gnd
SSyncB(input)	pin 15	pin 49 when sycbinsel = 1 else vcc
SSyncB(output)	auxout1 and pin 17	auxout1 and pin 17 when sycboutsel = 1
SWrReqB	pin 18	pin 14 when wrqboutsel = 0 else pin 9
SDtrReqB	pin 51 and pin 13	pin 51 and pin 17 when sycboutsel = 0
SRTSB	pin 48	pin 14 and pin 48
SCTSB	pin 46	pin 46
SDCDB	pin 11 when dcdbhfsel = 1 else pin 49	pin 49 when sycbinsel = 0 else gnd

PMC_SER_SW_IN

[0X04] PMC-SERIAL User Switch Port read only

USER CONTROL SWITCH REGISTER	
DATA BIT	DESCRIPTION
31-8	spare
7-0	UB7-UB0

FIGURE 5 PMC-SERIAL USER SWITCH READ PORT BIT MAP

The Switch Read Port has the eight user bits. These bits reflect the setting on the 8-position DIP switch on the PMC-Serial board. The switches allow custom configurations to be defined by the user such that the software will "know" how to configure a particular board in a multi-board system. The silk-screen is marked with the bit position and polarity definitions.

PMC_SER_INTSTAT

[0X08] PMC-SERIAL Status Port read only

STATUS	
DATA BIT	DESCRIPTION
31-24	spare
23	UART D Tx ready for data
22	UART C Tx ready for data
21	UART B Tx ready for data
20	UART A Tx ready for data
19	UART D Rx data ready
18	UART C Rx data ready
17	UART B Rx data ready
16	UART A Rx data ready
15	latched UART D interrupt
14	latched UART C interrupt
13	latched UART B interrupt
12	latched UART A interrupt
11	latched SCC interrupt
10	timer interrupt latch
8,9	spare
7	UART D interrupt in
6	UART C interrupt in
5	UART B interrupt in
4	UART A interrupt in
3	SCC interrupt in
2	spare
1	interrupt out
0	interrupt status

FIGURE 6 PMC-SERIAL STATUS PORT BIT MAP

Interrupt status when '1' indicates that an interrupt condition exists, however if the master interrupt enable is not asserted, then the interrupt will not be asserted onto the PCI bus. This bit can be used to operate the card in polled mode without interrupting the host.

Interrupt out when '1' indicates that an interrupt is asserted onto the PCI bus.

SCC interrupt in when '1' indicates that an interrupt condition exists on the SCC. This signal is used in the interrupt generation logic.

UART A-D interrupt in when '1' indicates that an interrupt condition exists on the corresponding UART channel. These signals are used in the interrupt generation logic.

Timer interrupt latch when '1' indicates that a timer interrupt has occurred. This bit must be cleared by writing a one to it (see figure 6 below). This is the signal used by the interrupt generation logic to create a system interrupt when a bus timeout occurs.

Latched SCC interrupt when '1' indicates that a SCC interrupt has occurred since the bit was last cleared by writing a one to it. The interrupt generation logic uses the unlatched bit directly from the SCC to create a system interrupt for the SCC. This bit is only used for informational purposes.

Latched UART A-D interrupt when '1' indicates that a UART interrupt has occurred on the corresponding channel since the bit was last cleared by writing a one to it. The interrupt generation logic uses the unlatched bit directly from the UART to create a system interrupt for the UART channel. These bits are only used for informational purposes.

UART A-D Rx data ready when '1' indicates that receive data is available to be read from the corresponding UART channel, when 'O' data is not available.

UART A-D Tx ready for data when '1' indicates that the corresponding channel is ready to accept Tx data, when 'O' the channel is not ready for data.

Latched UART A-D interrupt when '1' indicates that a UART interrupt has occurred on the corresponding channel since the bit was last cleared by writing a one to it. The interrupt generation logic uses the unlatched bit directly from the UART to create a system interrupt for the UART channel. These bits are only used for informational purposes.

UART A-D Rx data ready when '1' indicates that receive data is available to be read from the corresponding UART channel, when 'O' data is not available.

UART A-D Tx ready for data when '1' indicates that the corresponding channel is ready to accept Tx data, when 'O' the channel is not ready for data.

PMC_SER_IRUPT_CLR

[0X08] PMC-SERIAL SCC Interrupt Latch Clear Port write only

LATCH CLEAR	
DATA BIT	DESCRIPTION
15	clear UART D interrupt status latch
14	clear UART C interrupt status latch
13	clear UART B interrupt status latch
12	clear UART A interrupt status latch
11	clear SCC interrupt status latch
10	clear timer interrupt

FIGURE 7 PMC-SERIAL INTERRUPT/STATUS CLEAR BIT MAP

The above bits are latched high when the corresponding interrupt condition occurs. They will remain high until a one is written to the appropriate bit.

Note: Only the timer interrupt bit is required to be cleared when an interrupt is being serviced, the remaining latch bits are for status only.

PMC_SER_TERM

[0X10] PMC-SERIAL Termination Control Port read/write

CONTROL TERM REGISTER			
DATA BIT	DESCRIPTION		
31-16	spare		
15-0	termination	15-0	1 = terminated 0 = not terminated

FIGURE 8 PMC-SERIAL TERMINATION CONTROL BIT MAP

This register controls the termination of the 16 bi-directional IO lines. **Unused in the RTN5 version.**

PMC_SER_DIR

[0X14] PMC-SERIAL Direction Control Port read/write

CONTROL DIRECTION REGISTER			
DATA BIT	DESCRIPTION		
31-16	spare		
15-0	direction	15-0	0 = read 1 = drive

FIGURE 9 PMC-SERIAL DIRECTION CONTROL BIT MAP

This register controls the direction of the 16 bi-directional IO lines. When a one is written, the corresponding IO line is set to transmit, when the bit is a zero, the line is configured as a receiver. This register is overridden when the SCC is in full duplex mode. **Unused in RTN5 version**.

PMC_SER_DATA_SRC_422

[0X18] PMC-SERIAL IO Data Source Control Port read/write

CONTROL DATA SOURCE REGISTER		
DATA BIT	DESCRIPTION	
31-16	spare	
15-0	data source 15-0	1 = IO data register 0 = system

FIGURE 10 PMC-SERIAL RS-422 DATA SOURCE CONTROL BIT MAP

This register controls the data source for the 16 bi-directional IO lines when they are transmitting. When a one is written, the data is sourced from the IO data register, when zero, the system connections to the SCC drive the IO lines. In the RTN5 version there are 16 RS232 outputs and 16 RS232 inputs corresponding to this register. This register controls the TX RS232. These bits are the Alternate 422 IO and correspond to the SCC bits.

PMC_SER_DATA_422

[0X1C] PMC-SERIAL IO Data Port read/write

DATA REGISTER	
DATA BIT	DESCRIPTION
31-16	spare
15-0	RS-422 output data

FIGURE 11 PMC-SERIAL RS-422 TX DATA REGISTER BIT MAP

This register controls the data value for the 16 bi-directional IO lines when they are transmitting and the corresponding data source bit is enabled. For the RTN5 version the port controls the transmit side RS232. These bits are the Alternate 422 IO and correspond to the SCC bits.

PMC_SER_DATA_422RDBK

[0X20] PMC-SERIAL IO Data Read Port read only

DATA PORT	
DATA BIT	DESCRIPTION
31-16	spare
15-0	RS-422 input data

FIGURE 12 PMC-SERIAL RS-422 RX DATA PORT BIT MAP

This is the RS-422 data read-back port. When an IO line is configured as a receiver, the input data value can be read from this address. In the RTN5 version this port always reads back the 16 RS232 input port bits. These bits are the Alternate 422 IO and correspond to the SCC bits.

PMC_SER_DATA_SRC_232

[OX24] PMC-SERIAL RS-232 Data Source Control Port read/write

CONTROL DATA SOURCE REGISTER		
DATA BIT	DESCRIPTION	
31-10	spare	
9-8	data source TTL	1 = 232 data register 0 = SCC
7-0	data source 232	1 = 232 data register 0 = UART

FIGURE 13 PMC-SERIAL RS-232/TTL DATA SOURCE CONTROL REGISTER BIT MAP

This register controls the data source for the eight RS-232 output lines and the two auxiliary open drain TTL outputs. When a one is written, the data is sourced from the 232 data register, when zero, the system connections to the UART drive the RS-232 lines and the SCC syncA and B lines drive the TTL outputs.

PMC_SER_DATA_232

[OX28] PMC-SERIAL RS-232/TTL Data Port read/write

DATA REGISTER	
DATA BIT	DESCRIPTION
31-10	spare
9-8	TTL output data
7-0	RS-232 output data

FIGURE 14 PMC-SERIAL RS-232/TTL TX DATA REGISTER BIT MAP

This register controls the data value for the eight RS-232 output lines and the two auxiliary open drain TTL outputs when the corresponding data source bit is enabled.

PMC_SER_DATA_232RDBK

[OX2C] PMC-SERIAL RS-232/AUX Data Read Port read only

DATA PORT	
DATA BIT	DESCRIPTION
31-10	spare
9-8	AUX input data
7-0	RS-232 input data

FIGURE 15 PMC-SERIAL RS-232/AUX RX DATA PORT BIT MAP

This is the RS-232/AUX data read-back port. RS-232 and AUX0 and 1 input data values can be read from this address.

PMC_SER_TIMEOUT

[OX38] PMC-SERIAL Timeout Control Port read/write

This 16-bit register contains the pre-load count for the bus timeout counter. When a read from one of the UART Rx data ports occurs and the background read bit is enabled for that channel, the bus timeout counter will start counting down from this count. If the bus cycle does not complete before the count reaches zero, the bus cycle will be terminated with the timeout data specified in the next register. An interrupt will also occur provided the timer interrupt enable bit in the base control register has been set.

PMC_SER_TIMEOUT_DATA

[OX3C] PMC-SERIAL Timeout Data Port read/write

This 16-bit register contains the data value that will be returned when a bus timeout occurs as described above.

PMC_SER_CNTLA - D

[OX40 – OX4C] PMC-SERIAL UART Control Port read/write

CONTROL PORT

DATA BIT	DESCRIPTION
31-8	spare
7	enable 32-bit writes
6	enable 32-bit reads
5	enable 16-bit writes
4	enable 16-bit reads
3	enable background reads
2-1	spare
0	interrupt enable

FIGURE 16 PMC-SERIAL UART CONTROL REGISTER BIT MAP

Interrupt enable: When this bit is set to a one the interrupt is enabled for the corresponding UART channel, when this bit is a zero the interrupt is disabled.

Enable background reads: When this bit is set to a one the corresponding UART channel will monitor its RxReady line and will automatically read and store up to eight bytes of data that can be read immediately without further UART accesses. When this bit is a zero all data reads must wait for the UART to be accessed before returning.

Enable 16-bit reads: When this bit is set to a one 16-bit reads are enabled for the corresponding UART channel. If background reads are enabled, and sufficient data is stored, the data word will be put on the bus immediately. If background reads are not enabled two UART data read accesses will be executed before the bus cycle terminates.

Enable 16-bit writes: When this bit is set to a one 16-bit writes are enabled for the corresponding UART channel. The data will be latched and the bus

cycle will terminate immediately while two UART data write accesses are executed in the background. If another UART or SCC access is requested before this process completes, the new bus cycle will be delayed until the writes finish.

Enable 32-bit reads: When this bit is set to a one 32-bit reads are enabled for the corresponding UART channel. If background reads are enabled, and sufficient data is stored, the data word will be put on the bus immediately. If background reads are not enabled four UART data read accesses will be executed before the bus cycle terminates.

Enable 32-bit writes: When this bit is set to a one 32-bit writes are enabled for the corresponding UART channel. The data will be latched and the bus cycle will terminate immediately while four UART data write accesses are executed in the background. If another UART or SCC access is requested before this process completes, the new bus cycle will be delayed until the writes finish.

PMC_SER_SCC_A_CNTL

[OX88] PMC-SERIAL SCC Channel A Control Register read/write

This address is used to access every channel A register. In order to access a register other than this base register, the register number is first written to this address. A subsequent read or write will read from or write to the desired register. After this process has completed, the pointers are automatically reset to point to this base register. See the Z85230 documentation for more information on the process.

PMC_SER_SCC_A_DATA

[OX8C] PMC-SERIAL SCC Channel A Data Register read/write

This address is used to access the channel A data buffers. A write to this address loads a byte into the channel A transmit buffer, a read removes a byte from the receive buffer.

PMC_SER_SCC_B_CNTL

[OX90] PMC-SERIAL SCC Channel B Control Register read/write

This address is used to access every channel B register. In order to access a register other than this base register, the register number is first written to this address. A subsequent read or write will read from or write to the desired register. After this process has completed, the pointers are automatically reset to point to this base register is once again accessed. See the Z85230 documentation for more information on this process.

PMC_SER_SCC_B_DATA

[OX94] PMC-SERIAL SCC Channel B Data Register read/write

This address is used to access the channel B data buffers. A write to this address loads a byte into the channel B transmit buffer, a read removes a byte from the receive buffer.

PMC_SER_SCC_INTACK

[0XC0] PMC-SERIAL SCC Interrupt Acknowledge read only

This address is used to read the interrupt vector from the SCC. The intackn line is asserted for five clocks before the read line is asserted and the vector is driven onto the data bus. The SCC can be configured to put interrupt status in bits 4-6 or bits 1-3 of the vector which can be used to determine how to service the interrupt condition.

PMC_SER_QUART_A

[0X100] PMC-SERIAL UART A Base Address read/write

PMC_SER_QUART_B

[0X120] PMC-SERIAL UART A Base Address read/write

PMC_SER_QUART_C

[0X140] PMC-SERIAL UART A Base Address read/write

PMC_SER_QUART_D

[0X160] PMC-SERIAL UART A Base Address read/write

These are the base addresses of the four UART channels. In order to access a specific register add the offset of that register (see figure 3) to these base addresses. Note that some registers require certain bit patterns to be set up in other registers before they can be accessed. See the XR16C854 documentation for more detail on this process and the function of the various register bits.

Interrupts

PMC-Serial interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with a PMC-Serial interrupt the software must read the interrupt register to determine who caused the interrupt and process accordingly to clear the interrupt condition.

In order to clear the interrupt condition it will be necessary to access registers in the UART or the SCC to determine the particular cause of the interrupt, change the device interrupt enables, and service the device to remove the cause of the interrupt. The SCC can be configured so that the interrupt cause is read with an interrupt acknowledge/vector read cycle.

The interrupt level seen by the CPU is determined by the rest of the system. The master interrupt, the timer interrupt, and the SCC interrupt can be disabled or enabled through the PMC_SER_BASE register and the individual enables for the four UART channels are controlled by their respective control registers. In addition there are registers in the UART and SCC that must be configured for the particular conditions that are desired to generate an interrupt request.

An interrupt that is received from one of the UART channels or the SCC will

be latched into the PMC_SER_INTSTAT register, but this is only for status information. In order to reduce the number of bus accesses needed to process an interrupt, the interrupt signals coming directly from the UART and SCC are used in the interrupt logic. Therefore once the interrupting condition has been resolved on the UART or SCC the system interrupt will automatically be cleared. The latched bits in the PMC_SER_INTSTAT register do not need to be cleared if it is not convenient to do so.

The master enable is a mask that can be used to disable the interrupt from reaching the CPU, but still leaves the internal interrupt request hardware active for polled operation.

Power on initialization will provide a cleared interrupt request and interrupts disabled.

Loop-back

The Engineering kit has reference software, which includes external loop-back tests for the SCC and the UART through the Bezel connector. These tests require a PCI2PMC/PCIBPMC carrier board and an external cable connected to the 68-pin connector on the PMC-Serial-RTN5 with the following pins connected. UART A,B are RS422, UART C,D are RS232.

SIGNAL OUT	OUTPUT PIN	INPUT PIN	SIGNAL IN
U_TxA+	PIN-20	PIN-21	U_RxA+
U_TxA-	PIN-54	PIN-55	U_RxA-
U_TxB+	PIN-24	PIN-25	U_RxB+
U_TxB-	PIN-58	PIN-59	U_RxB-
U_TxC	PIN-26	PIN-22	U_RxC
U_RTSC	PIN-60	PIN-56	U_CTSC
U_TxD	PIN-27	PIN-23	U_RxD
U_RTSD	PIN-61	PIN-57	U_CTSD
AUXOUTO	PIN-63	PIN-29	AUXINO
AUXOUT1	PIN-64	PIN-30	AUXIN1
S_TxA	PIN-38	PIN-36	S_RxA
S_RTSA	PIN-39	PIN-37	S_CTSA
S_DTRA	PIN-42	PIN-40	S_DCDA
S_TRCA	PIN-43	PIN-7	S_RTCA
S_TxB	PIN-47	PIN-45	S_RxB
S_RTSB	PIN-48	PIN-46	S_CTSB
S_DTRB	PIN-51	PIN-49	S_DCDB
S_TRCB	PIN-52	PIN-16	S_RTCB

SCC operated in half duplex mode with dcd*hfsel = 0 and rtc*hfsel = 0 in the base control register.

PMC Serial RTN5 Front Panel IO

SIGNAL OUT		OUTPUT PIN	INPUT PIN	SIGNAL IN	
IN0	U_TXA+	PIN-20	PIN-21	U_RXA+	IN2
IN1	U_TXA -	PIN-54	PIN-55	U_RXA-	IN3
OUT_0	U_TXB+	PIN-24	PIN-25	U_RXB+	OUT_2
OUT_1	U_RXB-	PIN-58	PIN-59	U_RXB-	OUT_3
OUT_4	U_TXC	PIN-26	PIN-22	U_RXC	IN4
OUT_5	U_RTSC	PIN-60	PIN-56	U_CTSC	IN5
OUT_6	U_TXD	PIN-27	PIN-23	U_RXD	IN6
OUT_7	U_RTSD	PIN-61	PIN-57	U_CTSD	IN7
	AUXOUT0	PIN-63	PIN-29	AUXIN0	
	AUXOUT1	PIN-64	PIN-30	AUXIN1	
IO_2P	S_TXA/S_DTRA	PIN-4	PIN-36	S_RXA	IO_0N
IO_2N	S_TXA	PIN-38	PIN-2	S_DCDA	IO_0P
IO_3P	S_RTSA/S_WREQA	PIN-5	PIN-37	S_CTSA	IO_1N
IO_3N	S_RTSA	PIN-39	PIN-3	S_RTCA	IO_1P
IO_6P	S_DTRA/S_SYNCA	PIN-8	PIN-40	S_DCDA/S_SYNCA	IO_4N
IO_6N	S_DTRA	PIN-42	PIN-6	S_SYNCA	IO_4P
IO_7P	S_TRCA/S_WREQA	PIN-9	PIN-41	S_RTCA/S_TRCA	IO_5N
IO_7N	S_TRCA	PIN-43	PIN-7	S_RTCA	IO_5P
IO_10P	S_TXB/S_DTRB	PIN-13	PIN-45	S_RXB	IO_8N
IO_10N	S_TXB	PIN-47	PIN-11	S_DCDB	IO_8P
IO_11P	S_RTSB/S_WREQB	PIN-14	PIN-46	S_CTSB	IO_9N
IO_11N	S_RTSB	PIN-48	PIN-12	S_RTCB	IO_9P
IO_14P	S_DTRB/S_SYNCB	PIN-17	PIN-49	S_DCDB/S_SYNCB	IO_12N
IO_14N	S_DTRB	PIN-51	PIN-15	S_SYNCB	IO_12P
IO_15P	S_TRCB/S_WREQB	PIN-18	PIN-50	S_RTCB/S_TRCB	IO_13N
IO_15N	S_TRCB	PIN-52	PIN-16	S_RTCB	IO_13P
GND	A/C D/C OPEN	1,10,19,28 31	35,44,53 62,65,66,67,68		
3.3V	FUSED POWER	32			

FIGURE 17 PMC-SERIAL P1 INTERFACE

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-Serial. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 18 PMC-SERIAL PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-Serial-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 19 PMC-SERIAL PN2 INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC-Serial Module routed to Pn4. Also, see the User Manual for your carrier board for more information. **Please note that Pn4 is not installed on the RTN5 version**. The signals shown are for the base version of the design and could be connected for an RTN5 should rear IO be required. The signal names would be mapped from figure 17 to this one for the pin assignments.

IO_1+	IO_0+	1	2
IO_1-	IO_0-	3	4
IO_3+	IO_2+	5	6
IO_3-	IO_2-	7	8
IO_5+	IO_4+	9	10
IO_5-	IO_4-	11	12
IO_7+	IO_6+	13	14
IO_7-	IO_6-	15	16
IO_9+	IO_8+	17	18
IO_9-	IO_8-	19	20
IO_11+	IO_10+	21	22
IO_11-	IO_10-	23	24
IO_13+	IO_12+	25	26
IO_13-	IO_12-	27	28
IO_15+	IO_14+	29	30
IO_15-	IO_14- -	31	32
GND	GND	33	34
GND	GND	35	36
AUXIN0	AUXIN1	37	38
AUXOUT0	AUXOUT1	39	40
IN0	OUT0	41	42
IN1	OUT1	43	44
IN2	OUT2	45	46
IN3	OUT3	47	48
IN4	OUT4	49	50
IN5	OUT5	51	52
IN6	OUT6	53	54
IN7	OUT7	55	56
GND	GND	57	58
GND	3.3V REF	59	60
GND	3.3V REF	61	62
+6.5V REF	-6.5V REF	63	64

FIGURE 20 PMC-SERIAL PN4 INTERFACE

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. RS-232 and RS-485 interface devices provide some immunity from and allow operation when part of the circuit is powered on and part is not. It is better to avoid the issue of going past the safe operating areas by powering the equipment together and by having a good ground reference.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The PMC-Serial does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the PMC-Serial pin definitions. It is suggested that this standard cable be used for most of the cable run. The RTN5 version has mostly single ended signaling. Straight through untwisted pair cable is suitable for this version.

Terminal Block. We offer a high quality 68 screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68
[http://www.dyneng.com/HDEterm68.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the particular device's rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-Serial is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-Serial design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
support@dyneng.com

Specifications

Host Interface:	PCI Mezzanine Card
Serial Interfaces:	Four UART channels each with two RS232 drivers and receivers Two synchronous channels each with RS232 IO, one Mil. Std. 188-114A Type 1 enhanced hysteresis receiver for an external clock input, and one open drain TTL output for the sync out.
TX Data rates generated:	Up to 1.5 MHz for the UART channels. Up to 3.072 MHz for the SCC in synchronous mode. Other rates are available with different oscillator installations. Due to the RS-232 IO on the SCC the cable length may be limited at the higher rates.
Software Interface:	Control Registers, Status Ports, UART, and SCC Interface
Initialization:	Hardware reset forces all registers to 0, resets UART and SCC. Individual software resets for the UART and SCC.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses except UART and SCC accesses.
Interrupt:	Each UART channel has its own interrupt bit The SCC has one interrupt bit for both channels The interrupts generated by these devices depend on the setup specified in the UART and SCC internal registers
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	2.17 W/^{0}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC-Serial-RTN5	PMC Module with 4 UART channels[2-RS232, 2-RS422] and 2 synchronous/asynchronous serial channels Programmable baud rates Single ended data inputs and outputs RS-232 standard supported 32 bit data interface
Eng Kit–PMC-Serial	HDEterm68 - 68 position screw terminal adapter HDEcabl68 - 68 I0 twisted pair cable Technical Documentation, 1. PMC-Serial Schematic 2. PMC-Serial Reference test software Data sheet reprints are available from the manufacturer's web site reference software.
PMC-Serial-Driver	Windows 2000/XP compliant driver

***Note**: The Engineering Kit is strongly recommended for first time* PMC-Serial *buys.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.