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User Manual

ccPMC-HOTLink

Conduction-Cooled
Six-Channel HOTLink® Interface

Revision A
Corresponding Firmware: Revision A
Corresponding Hardware: 10-2009-0101

ccPMC-HOTLink
6-Channel HOTLink® Interface
Conduction-Cooled PMC Module

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Product Description

The PMC-HOTLink is part of the PMC Module family of modular I/O components by Dynamic Engineering. It features the Cypress Semiconductor CY7B923/CY7B933 HOTLink® Transmitter/Receiver pair. See the block diagram below:

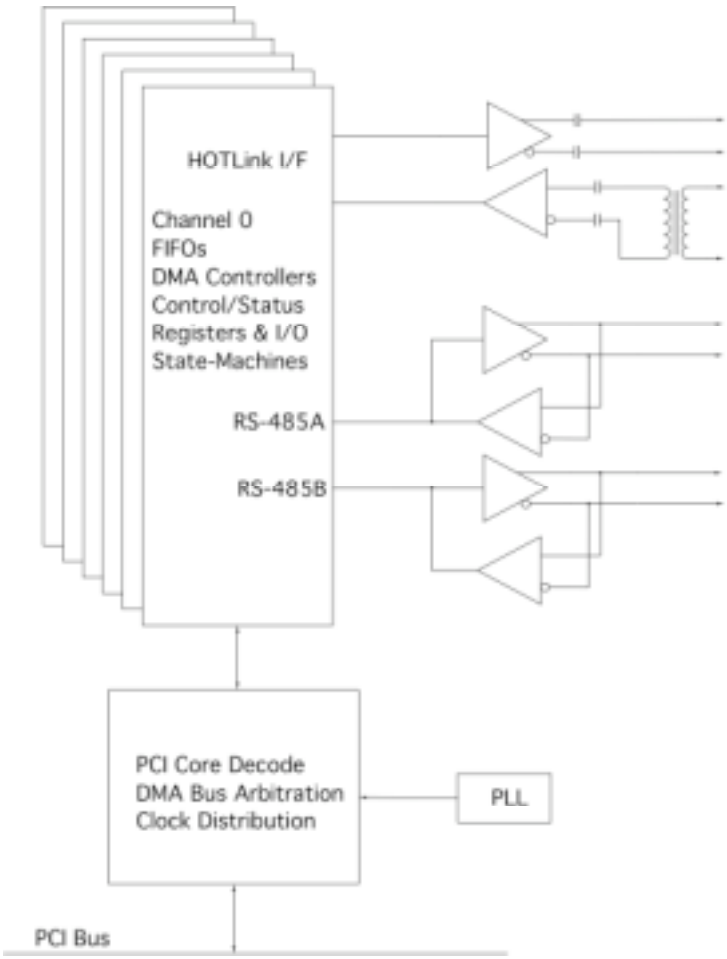

FIGURE 1 PMC-HOTLINK BLOCK DIAGRAM

The HOTLink protocol implemented provides positive emitter-coupled logic (PECL) data inputs and outputs. The transmit byte-rate is determined by the programmed frequency of the PLL clock A output. This clock is multiplied ten times by the HOTLink transmitter to send the transmit byte data-stream which is expanded to 10 bits by the internal 8B/10B encoder. The PLL is programmed via software over a serial I2C interface.

Six independent HOTLink channels are provided per card. Each HOTLink channel has four differential I/O signal pairs: A HOTLink differential PECL output, a HOTLink differential PECL input and two bi-directional differential RS-485 lines.

The HOTLink input is transformer-coupled into a dual 50 Ω termination referenced to 1.8 volts. The signals are then AC-coupled into the HOTLink receiver inputs referenced to 3.5 volt. The HOTLink output is AC-coupled after the bias/termination network and is present in this design for test purposes only.

The HOTLink receiver is supported by a 4k by 32-bit input data FIFO and the HOTLink transmitter has a 2k by 32-bit output data FIFO. These FIFOs can be accessed by single-word read/writes as well as DMA burst transfers. A FIFO test bit in each channel control register enables the data to be routed from the transmit to the receive FIFO for a full 32-bit path for loop-back testing of the FIFOs. Data is latched and the bus immediately released on a write-cycle. As soon as data is present in the FIFO it is pre-read to be immediately available for a read cycle. This allows minimal delay on the PCI write to transmit FIFO path and PCI read from the receive FIFO path as well as the accesses for the transmit and receive state machines.

Each channel also has two bi-directional RS-485 lines running an asynchronous 32-bit msb first protocol with low marking state. The 16x receive clock is supplied by the PLL clock A output. Each line is supported by a 1k by 32-bit FIFO that can be configured for either input or output use. Either line can be configured as a general purpose input or output, or setup to send data access requests at regular intervals (variable from 1.5 msec to about 3.5 msec in 2 usec increments) using a pre-defined 7-bit sync pattern. These requests trigger the output of a block of data that is received by the HOTLink receiver. The RS-485 FIFOs are only accessed using single-word transfers. Each FIFO can be directly written and read for FIFO testing or normal operation as either a receiver or transmitter.

This PMC module is conduction-cooled and has no front panel connector. All I/O connections are routed through PN4 and the PMC carrier to the outside world.

The PMC-HOTLink conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The PMC-HOTLink uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to

mate with the PMC-HOTLink, please let us know. We may be able to do a special build with a different height connector to compensate.

The received HOTLink data is written as long-words the receive FIFO. The first byte received is loaded into byte position zero (bits 7-0), the second byte goes in byte one (bits 15-8) and so on. If the receiver is disabled or at least sixteen consecutive Null bytes are received when a long-word has not been completed, the remaining unfilled bytes are set to zeros and the long-word is written to the receive FIFO.

Similarly the HOTLink transmitter reads long-words from the transmit FIFO and sends byte zero first followed by byte one, byte two and finally byte three.

The HOTLink board supports various interrupts. An interrupt can be configured to occur when the transmit FIFO is almost empty, the receive FIFO is almost full as well as various other events and error conditions. All interrupts are individually maskable and a channel master interrupt enable is provided to disable all interrupts on a channel simultaneously. The current real-time status is also available making it possible to operate in a polled mode.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

Theory of Operation

The PMC-HOTLink board is designed to interface with an electro-optic warning system. Commands are sent over an RS-485 line requesting an 8 Kbyte block of high-speed serial data which is collected by the HOTLink® receivers. This process is repeated 400 times a second.

The HOTLink board features a Spartan3-4000 Xilinx FPGA. The FPGA contains the PCI interface, all of the registers, FIFOs and protocol controlling elements of the HOTLink design. Only the transformers, HOTLink and RS-485 transceivers and clock circuitry are external to the Xilinx device.

A logic block within the Xilinx controls the PCI interface to the host CPU. The HOTLink design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather bus-master DMA is provided for in this design. Once the physical address of the first chaining descriptor is written to the DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block (only the lower 22 bits are valid). The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is set to one if the IO transfer is from the HOTLink board to host memory, and zero if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one. This process continues automatically until the last chaining descriptor in the list is processed.

The channel input and output DMA engines interface with the HOTLink transmit and receive FIFOs while the two RS-485 FIFOs are accessed by single-word transfers only. In normal operation, a command is sent over one of the channel’s two RS-485 lines once every 2.5 milliseconds (see Figure 2 below).

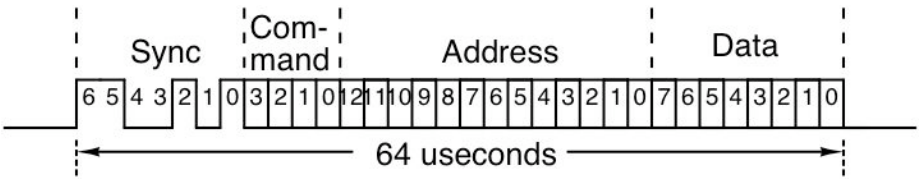

FIGURE 2 PMC-HOTLINK RS-485 COMMAND TIMING DIAGRAM

In response to this command the target system sends a frame of high-speed serial data at a rate of 170 Mbits/second (see Figure 3 below). This data has 8B/10B encoding with differential PECL signal levels. The data is received by the channel's HOTLink® receiver and stored in a 4k by 32-bit FIFO.

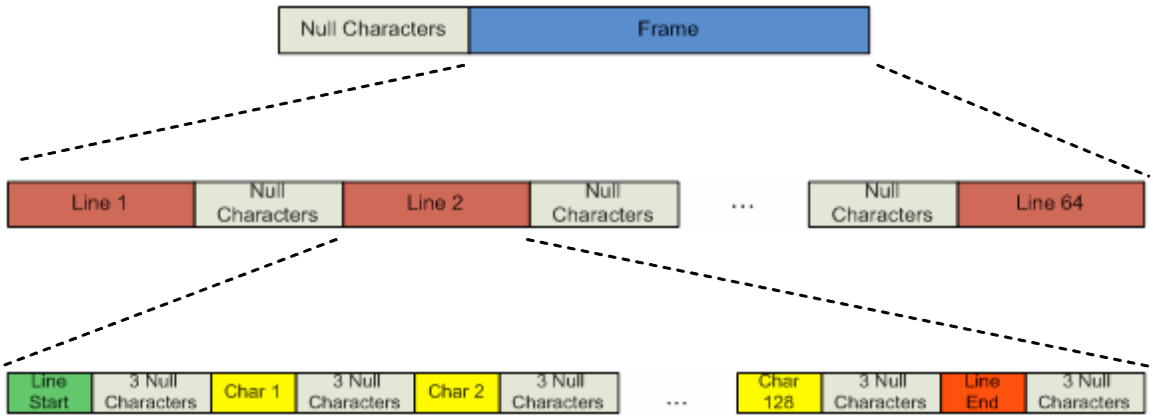

FIGURE 3 PMC-HOTLINK ELECTRO-OPTIC DATA-BLOCK STRUCTURE

Each PMC-HOTLink channel also has an onboard HOTLink transmitter. The transmitter is present for test purposes only and is connected to the receiver input B by an always-on internal link from output C. Also transmitter output A is AC-coupled to Pn4 for an external loop-back test connection to receiver input A.

The channel's second RS-485 line is used for testing, but it can also be used for a general purpose input or output. When an RS-485 transmitter is configured to send the data-frame requests, only the lower 25 bits of data from the FIFO are used, as the leading sync-pattern is predetermined and added automatically. The interval between frame requests is software adjustable from 1.5 to 3.5 milliseconds. When a transmitter is not configured for data-frame requests, the entire 32-bit word is read from the FIFO and sent on the line. Be sure to set bit 31 to a one when using the transmitter in this mode so the receiver will see the start-bit to recognize the beginning of the serial word.

Programming

Programming the PMC-HOTLink board requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the board is installed. The VendorId = 0x10EE. The CardId = 0x003A.

Depending on the software environment it may be necessary to set-up the system software with the PMC-HOTLink "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware. If DMA is to be used it will be necessary to acquire a block of non-paged memory that is accessible from the PCI bus in which to store chaining descriptor list entries. If the Dynamic Engineering device driver is used, the driver will handle all the DMA internal mechanics automatically.

In order to transmit or receive either HOTLink® or RS-485 data, the PLL must be programmed to the desired clock configuration. The PLL is connected to the Xilinx by an I^2C serial bus and its internal registers are loaded with 40 bytes of data that can be derived from a .jed file generated by the CyberClock utility from Cypress semiconductor http://www.dyneng.com/CyberClocks.zip. If you are using our driver, the PLL will be programmed to the default frequency settings when the driver initializes and can be read or re-programmed by an IOCTL call in the base driver.

Routines to use these calls to read and program the PLL are included in the UserApp code provided in the engineering kit for the board. If you are writing your own driver, contact Dynamic Engineering and we can send you a file with code excerpts from our driver and test software that cover each step of the process from parsing the .jed file to the low-level bit manipulation of the I_C bus.

In normal operation, the PMC-HOTLink sends data requests over one of the RS-485 I/O lines and waits to receive HOTLink data from the target system. This process is repeated 400 times per second. Data request data should be loaded into the appropriate RS-485 FIFO and the request timing interval set (this defaults to a 2.5 msec. delay if no other value is written). Once the relevant enables and configuration options are set, the board will wait to receive HOTLink data and store it in a 4K by 32-bit FIFO. The FIFO almost full level is programmable to whatever level is desired and once that level is reached, an interrupt will be asserted if it has been enabled. The data can then be read from the FIFO using DMA in an efficient manner.

All control characters are filtered-out of the data-stream, and 4-byte words containing only data values are written to the FIFO. When at least sixteen consecutive NULL characters are received and less than four bytes have been received since the last

FIFO write, the last partial word will be written to the FIFO with the unfilled bytes loaded with zeros.

Address Map

Register Name	Offset	Description
HLNK_BASE_CNTRL	0x0000	// Base Control register
HLNK_BASE_STATUS	0x0004	// Base Status read port
HLNK_CHAN_CNTRL_0	0x0010	// Channel 0 Control register
HLNK_CHAN_STATUS_0	0x0014	// Channel 0 Status register
HLNK_CHAN_FIFO_0	0x0018	// Channel 0 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_0	0x001C	// Channel 0 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_0	0x001C	// Channel 0 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_0	0x0020	// Channel 0 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_0	0x0020	// Channel 0 Receive FIFO data count
HLNK_CHAN_TX_AMT_0	0x0024	// Channel 0 TX almost empty level
HLNK_CHAN_RX_AFL_0	0x0028	// Channel 0 RX almost full level
HLNK_CHAN_485_CNTRL_0	0x002C	// Channel 0 RS-485 Control register
HLNK_CHAN_485_STATUS_0	0x0030	// Channel 0 RS-485 Status register
HLNK_CHAN_485A_FIFO_0	0x0034	// Channel 0 RS-485A FIFO port
HLNK_CHAN_485B_FIFO_0	0x0038	// Channel 0 RS-485B FIFO port
HLNK_CHAN_CNTRL_1	0x003C	// Channel 1 Control register
HLNK_CHAN_STATUS_1	0x0040	// Channel 1 Status register
HLNK_CHAN_FIFO_1	0x0044	// Channel 1 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_1	0x0048	// Channel 1 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_1	0x0048	// Channel 1 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_1	0x004C	// Channel 1 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_1	0x004C	// Channel 1 Receive FIFO data count
HLNK_CHAN_TX_AMT_1	0x0050	// Channel 1 TX almost empty level
HLNK_CHAN_RX_AFL_1	0x0054	// Channel 1 RX almost full level
HLNK_CHAN_485_CNTRL_1	0x0058	// Channel 1 RS-485 Control register
HLNK_CHAN_485_STATUS_1	0x005C	// Channel 1 RS-485 Status register
HLNK_CHAN_485A_FIFO_1	0x0060	// Channel 1 RS-485A FIFO port
HLNK_CHAN_485B_FIFO_1	0x0064	// Channel 1 RS-485B FIFO port
HLNK_CHAN_CNTRL_2	0x0068	// Channel 2 Control register
HLNK_CHAN_STATUS_2	0x006C	// Channel 2 Status register
HLNK_CHAN_FIFO_2	0x0070	// Channel 2 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_2	0x0074	// Channel 2 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_2	0x0074	// Channel 2 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_2	0x0078	// Channel 2 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_2	0x0078	// Channel 2 Receive FIFO data count
HLNK_CHAN_TX_AMT_2	0x007C	// Channel 2 TX almost empty level
HLNK_CHAN_RX_AFL_2	0x0080	// Channel 2 RX almost full level
HLNK_CHAN_485_CNTRL_2	0x0084	// Channel 2 RS-485 Control register
HLNK_CHAN_485_STATUS_2	0x0088	// Channel 2 RS-485 Status register
HLNK_CHAN_485A_FIFO_2	0x008C	// Channel 2 RS-485A FIFO port
HLNK_CHAN_485B_FIFO_2	0x0090	// Channel 2 RS-485B FIFO port

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HLNK_CHAN_CNTRL_3              0x0094  // Channel 3 Control register
HLNK_CHAN_STATUS_3             0x0098  // Channel 3 Status register
HLNK_CHAN_FIFO_3               0x009C  // Channel 3 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_3        0x00A0  // Channel 3 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_3      0x00A0  // Channel 3 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_3        0x00A4  // Channel 3 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_3      0x00A4  // Channel 3 Receive FIFO data count
HLNK_CHAN_TX_AMT_3             0x00A8  // Channel 3 TX almost empty level
HLNK_CHAN_RX_AFL_3             0x00AC  // Channel 3 RX almost full level
HLNK_CHAN_485_CNTRL_3          0x00B0  // Channel 3 RS-485 Control register
HLNK_CHAN_485_STATUS_3         0x00B4  // Channel 3 RS-485 Status register
HLNK_CHAN_485A_FIFO_3          0x00B8  // Channel 3 RS-485A FIFO port
HLNK_CHAN_485B_FIFO_3          0x00BC  // Channel 3 RS-485B FIFO port

HLNK_CHAN_CNTRL_4              0x00C0  // Channel 4 Control register
HLNK_CHAN_STATUS_4             0x00C4  // Channel 4 Status register
HLNK_CHAN_FIFO_4               0x00C8  // Channel 4 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_4        0x00CC  // Channel 4 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_4      0x00CC  // Channel 4 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_4        0x00D0  // Channel 4 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_4      0x00D0  // Channel 4 Receive FIFO data count
HLNK_CHAN_TX_AMT_4             0x00D4  // Channel 4 TX almost empty level
HLNK_CHAN_RX_AFL_4             0x00D8  // Channel 4 RX almost full level
HLNK_CHAN_485_CNTRL_4          0x00DC  // Channel 4 RS-485 Control register
HLNK_CHAN_485_STATUS_4         0x00E0  // Channel 4 RS-485 Status register
HLNK_CHAN_485A_FIFO_4          0x00E4  // Channel 4 RS-485A FIFO port
HLNK_CHAN_485B_FIFO_4          0x00E8  // Channel 4 RS-485B FIFO port

HLNK_CHAN_CNTRL_5              0x00EC  // Channel 5 Control register
HLNK_CHAN_STATUS_5             0x00F0  // Channel 5 Status register
HLNK_CHAN_FIFO_5               0x00F4  // Channel 5 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_5        0x00F8  // Channel 5 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_5      0x00F8  // Channel 5 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_5        0x00FC  // Channel 5 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_5      0x00FC  // Channel 5 Receive FIFO data count
HLNK_CHAN_TX_AMT_5             0x0100  // Channel 5 TX almost empty level
HLNK_CHAN_RX_AFL_5             0x0104  // Channel 5 RX almost full level
HLNK_CHAN_485_CNTRL_5          0x0108  // Channel 5 RS-485 Control register
HLNK_CHAN_485_STATUS_5         0x010C  // Channel 5 RS-485 Status register
HLNK_CHAN_485A_FIFO_5          0x0110  // Channel 5 RS-485A FIFO port
HLNK_CHAN_485B_FIFO_5          0x0114  // Channel 5 RS-485B FIFO port
```

FIGURE 4 PMC-HOTLINK REGISTER OFFSET ADDRESS MAP

Register Definitions

HLNK_BASE_CNTRL

[0x000] Base Control (read/write)

Base Control Register

Data Bit	Description
31-20	Spare
19	PLL sdata output
18	PLL s2 output
17	PLL sclk output
16	PLL Enable
15	Spare
14	Force Interrupt
13	Interrupt Enable
12-0	Spare

FIGURE 5 PMC-HOTLINK BASE CONTROL REGISTER

All bits are active high and are reset on system power-up or reset, except PLL enable, which defaults to enabled (high) on power-up or reset.

Interrupt enable: When this bit is set to a one all enabled interrupts for the referenced channel (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force interrupt: When this bit is set to a one a system interrupt will occur provided the channel master interrupt enable is set. This is useful to test interrupt service routines.

PLL Enable: When this bit is set to a one, the signals used to program and read the PLL are enabled.

PLL sclk/sdata output: These signals are used to program the PLL over the I_C serial interface. Sclk is always an FPGA output whereas sdata is bi-directional. When sdata is set to a one in this register, the PLL device can drive the sdata line to read back PLL register values. The value of the external sdata line is read from the HLNK_BASE_STATUS port defined below. When this register is read, the sdata value reflects the last value written to this control register. Please note that the reference rate of the PLL is set to 50 MHz.

PLL s2 output: This is an additional control line to the PLL that can be used to select additional pre-programmed frequencies.

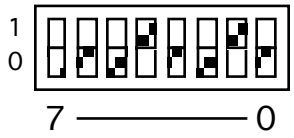
HLNK_BASE_STATUS

[0x004] Base Status Read – (read only)

Dipswitch Port	
Data Bit	**Description**
31	Interrupt Active
30-20	Spare
19	PLL sdata input
18-16	Spare
15-8	FPGA design revision number
7-0	Switch setting

FIGURE 6 PMC-HOTLINK BASE STATUS PORT

Sw7-0: The user switch is read through this port. The bits are read as the lowest byte. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Xilinx design revision number: The value of the second byte of this port is the rev. number of the Xilinx design (currently 0x00 – rev -).

PLL sdata input: The PLL_sdata bi-directional line is read using this bit. This line is used to read the register contents of the PLL.

Interrupt Active: When a one is read, it indicates that an enabled interrupt condition is active for the board. A zero indicates that no enabled interrupt condition is active.

HLNK_CHAN_CNTRL_0-5

[0x010, 0x03C, 0x068, 0x094, 0x0C0, 0x0EC] Channel Control (read/write)

Channel Control Register

Data Bit	Description
31-22	RS-485 Transmit Command Delay Adjust
21	Spare
20	HOTLink Receiver Reframe Enable
19	HOTLink Receiver BIT Enable
18	HOTLink Receiver Input A Select
17	HOTLink Transmitter ENN
16	HOTLink Transmitter Output Enable
15	HOTLink Transmitter BIT Enable
14	HOTLink Receiver Enable
13	HOTLink Transmitter Enable
12	HOTLink Transmit Test Enable
11	Read DMA Arbitration Priority Enable
10	Write DMA Arbitration Priority Enable
9	Read DMA Interrupt Enable
8	Write DMA Interrupt Enable
7	RX FIFO Overflow Interrupt Enable
6	RX FIFO Almost Full Interrupt Enable
5	TX FIFO Almost Empty Interrupt Enable
4	Force Interrupt
3	Master Interrupt Enable
2	FIFO Data Loop-Back Test Enable
1	Receive FIFO Reset
0	Transmit FIFO Reset

FIGURE 7 PMC-HOTLINK CHANNEL CONTROL REGISTER

All bits are active high and are reset on system power-up or reset. If an external control or status bit is active low, it is inverted from the value in this register.

Transmit/Receive FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO, packet length FIFO and control and status circuitry will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are referenced to the PCI clock; two periods are required for proper reset.

FIFO Data Loop-Back Test Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully

testing the data FIFOs without sending data to the HOTLink interface. When this bit is zero, normal FIFO operation is enabled.

Master interrupt enable: When this bit is set to a one all enabled interrupts for the referenced channel (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force interrupt: When this bit is set to a one a system interrupt will occur provided the channel master interrupt enable is set. This is useful to test interrupt service routines.

TX almost empty interrupt enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level is equal or less than the value specified in the HLNK_CHAN_TX_AMT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX almost full interrupt enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level is equal or greater to the value specified in the HLNK_CHAN_RX_AFL register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX FIFO Overflow Enable: When this bit is set to a one, an interrupt will be generated when an attempt is made to write to a full receive FIFO, provided the channel master interrupt enabled is asserted. When a zero is written to this bit, an interrupt will not be generated when an overflow condition occurs, but the latched status can still be read from the channel status register.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA write and read completion for the referenced channel. These two interrupts are not disabled by the master interrupt enable.

Write/Read DMA arbitration priority enable: These two bits, when set to one, enable the DMA arbiter to use the TX almost empty and/or RX almost full status to give priority to a channel that is approaching the limits of its FIFOs. The levels written to the TX almost empty and RX almost full registers are used to determine these status values. When these bits are zero normal round-robin arbitration is used to determine access to the PCI bus for DMA transfers.

HOTLink Transmit Test Enable: This bit, when set to one, enables transmitter test-mode operation. In this mode the transmit state-machine, if enabled, will read the transmit FIFO and send data bytes alternating with NULL bytes until the transmit data is exhausted. When this bit is zero, the transmit state-machine, when enabled, simulates the target system operation by waiting for a data request from the designated RS-485 input line and then sending 64 lines of 128 bytes each as described in the Theory or Operation section above.

HOTLink Transmitter Enable: This bit, when set to one, enables the HOTLink transmitter state-machine. The behavior of the transmitter depends on the state of the Test Enable bit described above, whether there is data in the FIFO and whether a data request is received from the RS-485 I/O. When this bit is zero, the transmitter state-machine is disabled.

HOTLink Receiver Enable: This bit, when set to one, enables the HOTLink receiver state-machine. The HOTLink receiver ignores control characters and stores only data bytes. Four bytes are loaded into a 32-bit long-word starting with the least significant byte and written to the receive FIFO. If a 32-bit word is not completed when the receiver is disabled or at least 16 consecutive NULL characters are received, the remaining unfilled byte positions will be set to zero and the word will be written to the FIFO. When this bit is zero, the receiver state-machine is disabled.

HOTLink Transmitter BIT Enable: This bit, when set to one, enables the HOTLink transmitter Built-In-Test mode. When this bit is zero, Built-In-Test mode is disabled.

HOTLink Transmitter Output Enable: This bit, when set to one, enables the external output of the HOTLink transmitter. When this bit is zero, only the internal output, which is always on, is enabled.

HOTLink Transmitter ENN: When the Built-In-Test mode is enabled, setting this bit to a one starts the test sequence. This bit is zero in normal operation.

HOTLink Receiver Input A Select: This bit, when set to one, selects input A on the HOTLink receiver. This input is driven by the transformer-coupled external input. When this bit is zero, input B is selected. This input is driven by the internal signal coming from the channel's HOTLink transmitter output C.

HOTLink Receiver BIT Enable: This bit, when set to one, enables the HOTLink receiver Built-In-Test mode. When this bit is zero, Built-In-Test mode is disabled.

HOTLink Receiver Reframe Enable: This bit, when set to one, asserts the HOTLink RF control line. This causes the HOTLink receiver chip to search for a comma character to align the serial bit-stream on a byte boundary. When this bit is zero, the RF control signal to the HOTLink receiver chip will be unasserted.

RS-485 Transmit Command Delay Adjust: This 10-bit field is used to adjust the delay between HOTLink data requests sent from the RS-485 transmitter. If this field is zero, a delay count of 500 will be added to the constant 750 to yield a delay of 1250 x 2 usec = 2.5 msec delay between commands issued. Any other value will be used as is and added to 750. Therefore the delay is adjustable from 1.502 msecs (for 1) to 3.546 msecs (for 0x3ff) in 2 usec increments.

HLNK_CHAN_STATUS_0-5

[0x014, 0x040, 0x06C, 0x098, 0x0C4, 0x0F0] Channel Status Read/Latch Clear Write

Channel Status Register

Data Bit	Description
31	Channel Interrupt Active
30	User Interrupt Active
29-22	Spare
23	RS-485B Framing Error
22	RS-485B Interrupt Active
21	RS-485A Framing Error
20	RS-485A Interrupt Active
19	Transmit Data Read
18	Receive Data Ready
17	Read DMA Ready (Idle)
16	Write DMA Ready (Idle)
15	Read DMA Error
14	Write DMA Error
13	Read DMA Complete
12	Write DMA Complete
11	Receive Symbol Error
10	Receive FIFO Overflow
9	Receive FIFO Almost Full Interrupt Active
8	Transmit FIFO Almost Empty Interrupt Active
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Transmit Data Valid
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 8 PMC-HOTLINK CHANNEL STATUS REGISTER

Transmit FIFO Empty: When a one is read, the transmit data FIFO for the corresponding channel contains no data; when a zero is read, there is at least one data-word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data-words in the transmit data FIFO for the corresponding channel is less than or equal to the value

written to the HLNK_CHAN_TX_AMT register for that channel; when a zero is read, the level is more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO for the corresponding channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Transmit Data Valid: When a one is read, there is at least one valid transmit data word left. This bit can be set even if the transmit FIFO is empty, because there is a one-word pipeline after the FIFO output to feed the transmit I/O or FIFO bypass path. When this bit is a zero, it indicates that there is no more valid transmit data.

Receive FIFO Empty: When a one is read, the receive data FIFO for the corresponding channel contains no data; when a zero is read, there is at least one data-word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data-words in the receive data FIFO for the corresponding channel is greater or equal to the value written to the HLNK_CHAN_RX_AFL register for that channel; when a zero is read, the level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO for the corresponding channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Receive Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO status reports empty, because there is a four-word pipeline after the FIFO output to facilitate a PCI read DMA. When this bit is a zero, it indicates that there is no more valid receive data.

Transmit FIFO Almost Empty Interrupt Active: When a one is read, it indicates that the transmit FIFO data count has become less than or equal to the value in the HLNK_CHAN_TX_AMT register. A zero indicates that the FIFO has not become almost empty. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive FIFO Almost Full Interrupt Active: When a one is read, it indicates that the receive FIFO data count has become greater than or equal to the value in the HLNK_CHAN_RX_AFL register. A zero indicates that the FIFO has not become almost full. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive FIFO Overflow: When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. A zero indicates that no overflow condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Symbol Error: This is a latched version of the RVS (Received Violation Symbol) signal from the channel's HOTLink receiver. This bit is intended to be used for Built-In-Test operation as it indicates an error during the test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Write/Read DMA Complete: When a one is read, it indicates that the corresponding DMA has completed. These bits are latched and must be cleared by writing the same bit back to this channel status port. A zero indicates that the corresponding DMA has not transitioned from running to completed since the bit was last cleared.

Write/Read DMA Error: When a one is read, it indicates that an error has occurred while the corresponding DMA was in progress. This could be a target or master abort or an incorrect direction bit in one of the DMA descriptors. These bits are latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no DMA error has occurred.

Write/Read DMA ready (Idle): These two bits report the DMA state-machine status. If a one is read, the corresponding DMA state-machine is idle and available to start a transfer. If a zero is read, the corresponding DMA state-machine is already processing a data transfer.

Receive Data Ready: This is a latched version of the ready signal from the channel's HOTLink receiver. This bit is intended to be used for Built-In-Test operation as the ready signal will pulse once per test loop, so polling this bit will indicate the completion of the receive test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Transmit Data Read: This is a latched version of the data read signal from the channel's HOTLink transmitter. Similarly to the ready bit above, this bit is intended to be used for Built-In-Test operation as the data read signal will pulse once per test loop, so polling this bit will indicate the completion of the transmit test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

RS-485A/B Interrupt Active: When a one is read, it indicates that the corresponding RS-485 state-machine has completed its operation since the bit was last cleared. A zero indicates that this has not occurred. This bit is latched and must be cleared by writing the same bit back to the channel status port.

RS-485A/B Framing Error: When a one is read, it indicates that the corresponding RS-485 receiver state-machine has detected a framing error since the bit was last cleared. A framing error occurs if the 33rd bit (stop-bit) of a transmitted word is high, or if the receiver is in command mode and the 7-bit sync pattern at the beginning of the word is

incorrect. A zero indicates that this has not occurred. This bit is latched and must be cleared by writing the same bit back to the channel status port.

User Interrupt Active: When a one is read, it indicates that an enabled user interrupt condition (other than the DMA interrupts) is active for the referenced channel. A zero indicates that no enabled interrupt condition is active.

Channel Interrupt Active: When a one is read, it indicates that the interrupt is active for the referenced channel. A zero indicates that the channel interrupt is active.

HLNK_CHAN_FIFO_0-5

[0x018, 0x044, 0x070, 0x09C, 0x0C8, 0x0F4] TX FIFO Write/RX FIFO Read

RX and TX FIFO Ports

Data Bit	Description
31-0	FIFO data word

FIGURE 9 PMC-HOTLINK CHANNEL RX/TX FIFO PORT

These ports are used to make single-word accesses into the channel transmit FIFO and out of the channel receive FIFO.

HLNK_CHAN_WR_DMA_PNTR_0-5

[0x01C, 0x048, 0x074, 0x0A0, 0x0CC, 0x00F8] Input DMA Control (write only)

Input DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 10 PMC-HOTLINK CHANNEL WRITE DMA POINTER PORT

This write-only port is used to initiate a scatter-gather input DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block (only the lower 22 bits are valid), and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values.

HLNK_CHAN_TX_FIFO_COUNT_0-5

[0x01C, 0x048, 0x074, 0x0A0, 0x0CC, 0x0F8] TX FIFO Word Count (read only)

TX FIFO Data Count	
Data Bit	**Description**
31-12	Spare
11-0	TX data words stored

FIGURE 11 PMC-HOTLINK CHANNEL TX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding transmit FIFO. There is an additional latch that may contain data if enabled, which allows this value to be a maximum of 0x801.

HLNK_CHAN_RD_DMA_PNTR_0-5

[0x020, 0x04C, 0x078, 0x0A4, 0x0D0, 0x0FC] Output DMA Control (write only)

Output DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 12 PMC-HOTLINK CHANNEL READ DMA POINTER PORT

This write-only port is used to initiate a scatter-gather output DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block (only the lower 22 bits are valid), and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values.

HLNK_CHAN_RX_FIFO_COUNT_0-5

[0x020, 0x04C, 0x078, 0x0A4, 0x0D0, 0x0FC] RX FIFO Word Count (read only)

RX FIFO Data Count	
Data Bit	**Description**
31-12	Spare
11-0	RX data words stored

FIGURE 13 PMC-HOTLINK CHANNEL RX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding receive FIFO. There are four additional latches in the read DMA pipeline that may contain data, which allows this value to be a maximum of 0x1004.

HLNK_CHAN_TX_AMT_0-5

[0x024, 0x050, 0x07C, 0x0A8, 0x0D4, 0x100] TX FIFO Almost Empty Level (read/write)

TX FIFO Almost Empty Level Register

Data Bit	Description
31-16	Spare
15-0	TX FIFO almost empty level

FIGURE 14 PMC-HOTLINK CHANNEL TX FIFO AMT LEVEL REGISTER

These read/write ports access the transmitter almost-empty level registers for the respective channels. When the number of data words in the transmit data FIFO is equal or less than this value, the almost empty status bit is set and an interrupt may be generated if it is enabled.

HLNK_CHAN_RX_AFL_0-5

[0x028, 0x054, 0x080, 0x0AC, 0x0D8, 0x104] RX FIFO Almost Full Level (read/write)

RX FIFO Almost Full Level Register

Data Bit	Description
31-16	Spare
15-0	RX FIFO almost full level

FIGURE 15 PMC-HOTLINK CHANNEL RX AFL LEVEL REGISTER

These read/write ports access the receiver almost-full level registers for the respective channels. When the number of data words in the receive data FIFO is equal or greater than this value, the almost full status bit is set and an interrupt may be generated if it is enabled.

HLNK_CHAN_485_CNTRL_0-5

[0x02C, 0x058, 0x084, 0x0B0, 0x0DC, 0x108] Channel RS-485 Control (read/write)

Channel RS-485 Control Register

Data Bit	Description
31-26	Spare
25	RS-485B TX Load Enable
24	RS-485B I/O Enable
23	Spare
22	RS-485B Delay Count Enable
21	RS-485B Command Enable
20	RS-485B Interrupt Enable
19	RS-485B Start/Load Clear Enable
18	RS-485B Direction (1=Transmit, 0=Receive)
17	RS-485B Termination Enable
16	RS-485B FIFO Reset
15-10	Spare
9	RS-485A TX Load Enable
8	RS-485A I/O Enable
7	Spare
6	RS-485A Delay Count Enable
5	RS-485A Command Enable
4	RS-485A Interrupt Enable
3	RS-485A Start/Load Clear Enable
2	RS-485A Direction (1=Transmit, 0=Receive)
1	RS-485A Termination Enable
0	RS-485A FIFO Reset

FIGURE 16 PMC-HOTLINK CHANNEL RS-485 CONTROL REGISTER

All bits are active high and are reset on system power-up or reset.

RS-485A/B FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are referenced to the PCI clock; two periods are required for proper reset.

RS-485A/B Termination Enable: When this bit is set to a one, the parallel termination for the selected RS-485 I/O line will be switched in. When a zero is written to this bit, the corresponding parallel termination will remain open.

RS-485A/B Direction (1=Transmit, 0=Receive): When this bit is set to a one, the selected RS-485 I/O line will be configured as a transmitter. When a zero is written to this bit, the selected RS-485 I/O line will be configured as a receiver.

RS-485A/B Start/Load Clear Enable: When this bit is set to a one, the I/O enable and TX load enable bits will be cleared when the state-machine completes its current data reception or data transmission operation. When a zero is written to this bit, the enable bits will not be cleared on completion, but the interrupt status bit will still be latched.

RS-485A/B Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the selected state-machine completes its current data reception or data transmission operation, provided the channel master interrupt enabled is asserted. When a zero is written to this bit, an interrupt will not be generated, but the latched status can still be read from the channel status register.

RS-485A/B Command Enable: When this bit is set to a one, the selected RS-485 I/O line will be . When a zero is written to this bit,

RS-485A/B Delay Count Enable: When this bit is set to a one and the command enable bit is set and the selected RS-485 I/O line is configured as a transmitter, . When a zero is written to this bit,

RS-485A/B I/O Enable: When this bit is set to a one, the referenced state-machine is enabled. If the direction bit is set to one, the transmit state-machine is enabled and if the direction bit is zero, the receive state-machine is enabled. When a zero is written to this bit, neither state-machine is enabled.

RS-485A/B TX Load Enable: When this bit is set to a one and the selected RS-485 I/O line is configured as a transmitter, data loading from the corresponding FIFO is enabled. When a zero is written to this bit or the selected RS-485 I/O line is configured as a receiver, data present in the corresponding FIFO will not be read and loaded into the I/O state-machine.

HLNK_CHAN_485_STATUS_0-5

[0x030, 0x05C, 0x088, 0x0B4, 0x0E0, 0x10C] Channel RS-485 Status read/Clear write

Channel RS-485 Status Register

Data Bit	Description
31	Spare
30	Spare
29-20	RS-485B FIFO Word Count
19	Spare
18	RS-485B FIFO Data Valid
17	RS-485B FIFO Full
16	RS-485B FIFO Empty
15	Spare
14	Spare
13-4	RS-485A FIFO Word Count
3	Spare
2	RS-485A FIFO Data Valid
1	RS-485A FIFO Full
0	RS-485A FIFO Empty

FIGURE 17 PMC-HOTLINK CHANNEL RS-485 STATUS REGISTER

RS-485A/B FIFO Empty: When a one is read, the referenced RS-485 data FIFO for the corresponding channel contains no data; when a zero is read, there is at least one data-word in the FIFO.

RS-485A/B FIFO Full: When a one is read, the referenced RS-485 data FIFO for the corresponding channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

RS-485A/B FIFO Data Valid: When a one is read, there is at least one valid RS-485 data word left. This bit can be set even if the RS-485 FIFO is empty, because there is a one-word pipeline after the FIFO output. When this bit is a zero, it indicates that there is no more valid RS-485 data.

RS-485A/B FIFO Word Count: This 10-bit field reports the referenced RS-485 FIFO word count.

HLNK_CHAN_485A/B_FIFO_0-5

[0x034, 0x060, 0x08C, 0x0B8, 0x0E4, 0x110] RS-485A FIFO (read/write)

[0x038, 0x064, 0x090, 0x0BC, 0x0E8, 0x114] RS-485B FIFO (read/write)

RS-485A/B FIFO Port	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 18 PMC-HOTLINK CHANNEL RS-485A FIFO PORT

These ports are used to make single-word accesses in and out of the two channel RS-485 FIFOs.

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-HOTLink. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 19 PMC-HOTLINK PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-HOTLink. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 20 PMC-HOTLINK PN2 INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC-HOTLink Module Pn4. Also, see the User Manual for your carrier board for information on interfacing with Pn4.

HSSIN_0+	HSSIN_1+	1	2
HSSIN_0-	HSSIN_1-	3	4
HSSIN_2+	HSSIN_3+	5	6
HSSIN_2-	HSSIN_3-	7	8
HSSIN_4+	HSSIN_5+	9	10
HSSIN_4-	HSSIN_5-	11	12
DEBUG+	IO_0+	13	14
DEBUG-	IO_0-	15	16
IO_1+	IO_2+	17	18
IO_1-	IO_2-	19	20
IO_3+	IO_4+	21	22
IO_3-	IO_4-	23	24
IO_5+	IO_6+	25	26
IO_5-	IO_6-	27	28
IO_7+	IO_8+	29	30
IO_7-	IO_8-	31	32
IO_9+	IO_10+	33	34
IO_9-	IO_10-	35	36
IO_11+		37	38
IO_11-		39	40
		41	42
		43	44
HSSOUT_0+	HSSOUT_1-	45	46
HSSOUT_0-	HSSOUT_1+	47	48
HSSOUT_2+	HSSOUT_3-	49	50
HSSOUT_2-	HSSOUT_3+	51	52
HSSOUT_4+	HSSOUT_5-	53	54
HSSOUT_4-	HSSOUT_5+	55	56
		57	58
		59	60
		61	62
		63	64

FIGURE 21 PMC-HOTLINK PN4 INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-HOTLink. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-HOTLink is constructed out of 0.062-inch thick FR4 material.

Through-hole and surface-mount components are used. IC sockets use screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-HOTLink design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. The board is conduction-cooled, therefore low thermal impedance to the carrier cooling rails and surfaces is imperative. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Host Interface (PMC):	PCI Mezzanine Card
Serial Interfaces:	Six HOTLink inputs and six HOTLink outputs Twelve RS-485 bi-directional lines
TX Bit-rates generated:	170 MHz for the HOTLink I/O, 500 kHz for the RS-485 I/O Frequencies can be varied by reprogramming the PLL
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	Each channel has an interrupt for TX almost empty, RX almost full, RX FIFO overflow, RS-485A/B I/O complete. Read and write DMA interrupts are also implemented for each channel.
DMA:	Independent input and output Scatter/Gather DMA Support implemented for each channel
Onboard Options:	All Options are Software Programmable
Interface Options:	All HOTLink and RS-485 I/O lines are available on Pn4 only
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC-HOTLink	http://www.dyneng.com/pmc_hotlink.html Standard version with one 4K x 32-bit FIFO, one 2K x 32-bit FIFO and two 1K x 32-bit FIFOs per channel. Six channels, I/O on Pn4.
PMC-HOTLink-Eng-1	Engineering Kit for the PMC-HOTLink board-level schematics (PDF)
PMC-HOTLink-Eng-2	Board-level schematics (PDF), Linux Driver and sample application
PMC-HOTLink-Eng-3	Board-level schematics (PDF), Windows Driver and sample application