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User Manual

PMC-Wizard

Two-Channel Wizard Interface

Revision B1
Corresponding Hardware: Revision A
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Corresponding Firmware: Revision B

PMC-Wizard
PMC based 2-Channel
WizardLink Interface

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Product Description

The PMC-Wizard is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-Wizard uses two TLK2711 transceivers from Texas Instruments to implement the two high-speed serial interfaces. The TLK2711 is a member of the *WizardLink* transceiver family of multigigabit transceivers, intended for use in ultrahigh-speed bidirectional point-to-point data transmission systems.

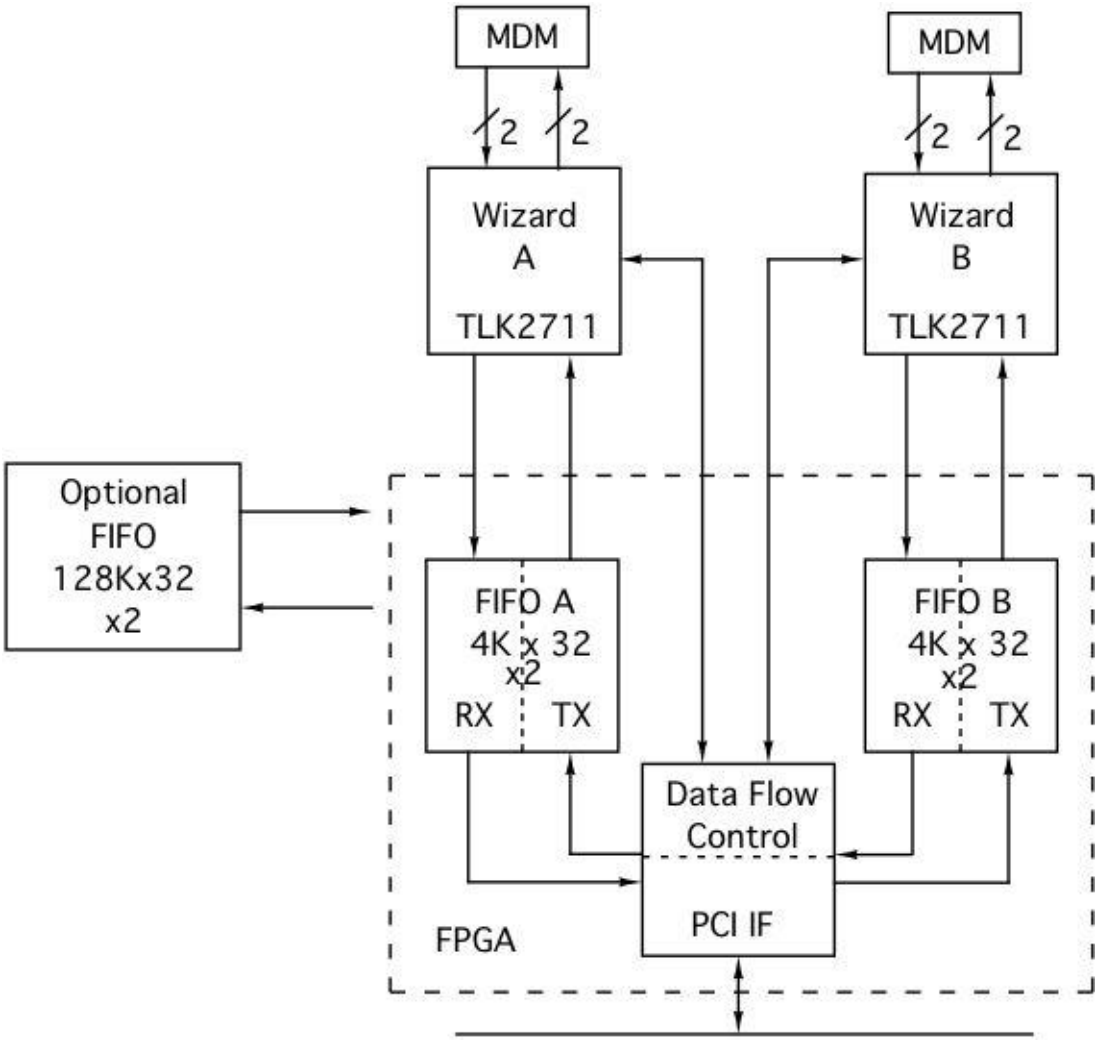


FIGURE 1 PMC-WIZARD BLOCK DIAGRAM

All configuration registers support read and write operations for maximum software convenience. All addresses are long word (32-bit) aligned.

The PMC-Wizard conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system

prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The PMC-Wizard uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the PMC-Wizard, please let us know. We may be able to do a special build with a different height connector to compensate.

Theory of Operation

The PMC Wizard is designed for transferring parallel data from one point to another using the WizardLink protocol. This protocol translates 16 bits of parallel data into 20 bits of serial data using 8-bit/10-bit encoding and sends it across a differential pair serial line at 20 times the rate that the parallel data is clocked into the Wizard device. At the receiving end the signal is decoded and restored to 16-bit parallel data.

Data is sent as 4104 byte messages. The first four bytes are the sync pattern (header) used by the receiver to detect the beginning of a message. The last four bytes make up the trailer. The header and trailer are written to the transmitter, but only the 4096-byte message body is stored to the receive FIFO. The data is written to and read from the PCI bus as 32-bit words. Each word is sent and received lower half first, then upper half. Between each message a minimum of two 16-bit idle patterns are sent.

The PMC Wizard features a Xilinx FPGA. The FPGA contains all of the registers, FIFOs and protocol controlling elements of the PMC-Wizard design. Only the Wizard chips and PLL circuit are external to the Xilinx device.

The PMC-Wizard is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. In standard configuration, the PMC-Wizard is a Type 1 mechanical with only low profile passive components on the back of the board, one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and basic logic design.
A logic block within the Xilinx controls the PCI interface to the host CPU. The PMC-Wizard design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather DMA is supported by two input and two output DMA engines. Once the physical address of the first chaining descriptor is written to one of the DMA pointer registers, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is set to one if the IO transfer is from the PMC Wizard board to host memory, and zero if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

The four DMA engines can all operate simultaneously. PCI bus access is arbitrated on a round-robin basis with a DMA engine relinquishing the bus at the end of each list entry transfer or when the corresponding FIFO gets close to full for the transmit or empty for the receive.

Programming

Programming the PMC-Wizard requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed. The VendorId = 0x10EE. The CardId = 0x0023. Current revision = 0x02

Depending on the software environment it may be necessary to set-up the system software with the PMC-Wizard "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

If DMA is to be used it will be necessary to acquire a block of non-paged memory that is accessible from the PCI bus in which to store chaining descriptor list entries. After the list entries are stored in the non-paged memory block, the address of the first list entry is written to one of the DMA engines to begin DMA processing. The DMA continues until the list is complete and an interrupt is signaled to clean-up the transfer and potentially begin another. It is necessary that all memory pages that are to be accessed be physically resident in memory while the DMA is in progress.

Address Map

Register Name	Offset	Description
PMC_WIZ_BASE	0x0000	// Base control register
PMC_WIZ_USER_SWITCH	0x0004	// User switch/Xilinx rev. read port
PMC_WIZ_INT_STATUS	0x0008	// Interrupt status/clear port
WIZ_CHAN0_CNTRL	0x0010	// Channel 0 Control register offset
WIZ_CHAN0_STATUS	0x0014	// Channel 0 Status read/latch clear port offset
WIZ_CHAN0_WR_DMA_PNTR	0x0018	// Channel 0 Write DMA physical address register
WIZ_CHAN0_RD_DMA_PNTR	0x001C	// Channel 0 Read DMA physical address register
WIZ_CHAN0_FIFO	0x0020	// Channel 0 FIFO offset for single word access
WIZ_CHAN0_RX_AFL_LVL	0x0024	// Channel 0 RX almost full level register offset
WIZ_CHAN0_TX_AMT_LVL	0x0028	// Channel 0 TX almost empty level register offset
WIZ_CHAN0_TX_FIFO_COUNT	0x002C	// Channel 0 TX FIFO count read port offset
WIZ_CHAN0_RX_FIFO_COUNT	0x0030	// Channel 0 RX FIFO count read port offset
WIZ_CHAN0_SYNC_PATTERN	0x0034	// Channel 0 RX Sync pattern
WIZ_CHAN0_IDLE_CONFIG	0x0038	// Channel 0 TX Idle pattern and count
WIZ_CHAN1_CNTRL	0x0040	// Channel 1 Control register offset
WIZ_CHAN1_STATUS	0x0044	// Channel 1 Status read/latch clear port offset
WIZ_CHAN1_WR_DMA_PNTR	0x0048	// Channel 1 Write DMA physical address register
WIZ_CHAN1_RD_DMA_PNTR	0x004C	// Channel 1 Read DMA physical address register
WIZ_CHAN1_FIFO	0x0050	// Channel 1 FIFO offset for single word access
WIZ_CHAN1_RX_AFL_LVL	0x0054	// Channel 1 RX almost full level register offset
WIZ_CHAN1_TX_AMT_LVL	0x0058	// Channel 1 TX almost empty level register offset
WIZ_CHAN1_TX_FIFO_COUNT	0x005C	// Channel 1 TX FIFO count read port offset
WIZ_CHAN1_RX_FIFO_COUNT	0x0060	// Channel 1 RX FIFO count read port offset
WIZ_CHAN1_SYNC_PATTERN	0x0064	// Channel 1 RX Sync pattern
WIZ_CHAN1_IDLE_CONFIG	0x0068	// Channel 1 TX Idle pattern and count

FIGURE 2 PMC-WIZARD XILINX ADDRESS MAP

Register Definitions

PMC_WIZ_BASE

[0x0000] Base Control Register (read/write)

Base Control Register

Data Bit	Description
31-20	Spare
19	PLL SDAT Output
18	PLL S2 Output
17	PLL SCLK Output
16	PLL Enable
15-2	Spare
1	Force Interrupt
0	Master Interrupt Enable

FIGURE 3 PMC-WIZARD BASE CONTROL REGISTER

All bits are active high and are reset on power-up or reset command, except PLL Enable, which defaults to enabled (high) on power-up or reset.

Master Interrupt Enable: When this bit is set to a one all local interrupts will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host. Currently the only interrupt source for this portion of the design is the Force Interrupt bit.

Force Interrupt: When this bit is set to a one a system interrupt will occur provided the Master Interrupt Enable is set. This is useful for software development and debugging.

PLL Enable: When this bit is set to a one, the signals used to program and read the PLL are enabled.

PLL SCLK / SDAT Output: These signals are used to program the PLL over the I2C serial interface. SCLK is always an output whereas SDAT is bi-directional. This is where the SDAT output value is specified. When SDAT is an input it is read from the User Switch Port.

PLL S2 Output: This is an additional control line to the PLL that can be used to select alternative pre-programmed frequencies.

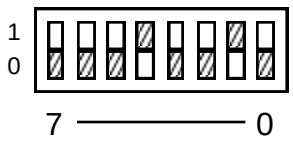
PMC_WIZ_USER_SWITCH

[0x0004] User Switch Port (read only)

Dip-Switch Port	
Data Bit	**Description**
31-20	Spare
19	PLL SDAT Input
18-16	Spare
15-8	Xilinx Design Revision Number
7-0	Sw7-0

FIGURE 4 PMC-WIZARD USER SWITCH PORT

Sw7-0: The user switch is read through this read-only port. The bits are read as the lowest byte. Access the port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Xilinx Design Revision Number: The value of the second byte of this port is the rev. number of the Xilinx design (currently 0x02 - rev. B).

PLL SDAT Input: This is where the PLL data line is read when data is being read from the PLL. This line is used to read the register contents of the PLL.

PMC_WIZ_STATUS
[0x0008] Status Register (read only)

Status Register	
Data Bit	**Description**
31	Interrupt Status
30-2	Spare
1	Transmit Clock Locked
0	Local Interrupt Active

FIGURE 5 PMC-WIZARD STATUS REGISTER

Local Interrupt Active: When read as a '1', a local interrupt condition is active. Currently, the only such condition is the Force Interrupt bit in the Base Control Register. A system interrupt will not occur unless the Master Interrupt Enable bit in the Base Control Register is also set. When read as a '0', no local interrupt conditions are active.

Transmit Clock Locked: When read as a '1', this bit indicates that the transmit clock generator is locked. A lock detect/clock generator reset circuit is implemented in hardware to insure that the lock is achieved and maintained. When read as a '0', it indicates that the clock generator is not locked. This would most likely be caused by the absence of an input clock from the PLL.

Interrupt Status: When read as a '1', an enabled local interrupt condition is active and a system interrupt should be asserted. When read as a '0', no enabled local interrupt is active.

WIZ_CHAN0/1_CNTRL

[0x0010, 0x0040] Channel Control Register (read/write)

Control Register

Data Bit	Description
31-19	Spare
18	Sync Disable
17	TX Almost Empty Interrupt Enable
16	RX Almost Full Interrupt Enable
15	RX Overflow Interrupt Enable
14	RX Interrupt Enable
13	TX Interrupt Enable
12	RX Enable
11	TX Enable
10	PRBS Enable
9	Lock Reference Enable
8	Internal Loop-back Enable
7	Pre-emphasis Enable
6	IO Enable
5	Force Interrupt
4	Master Interrupt Enable
3	DMA Read Enable
2	DMA Write Enable
1	FIFO Bypass Enable
0	FIFO Reset

FIGURE 6 PMC-WIZARD CHANNEL CONTROL REGISTER

FIFO Reset: When this bit is set to a one, the transmit and receive FIFOs for the referenced channel will be reset. When this bit is zero, normal FIFO operation is enabled.

FIFO Bypass Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without going through the Wizard chip. When this bit is zero, normal operation is enabled.

DMA Write Enable: When this bit is set to a one, the write DMA interrupt is enabled for the referenced channel. When this bit is zero, the write DMA interrupt is disabled.

DMA Read Enable: When this bit is set to a one, the read DMA interrupt is enabled for the referenced channel. When this bit is zero, the read DMA interrupt is disabled.

Master Interrupt Enable: When this bit is set to a one, all enabled interrupts will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one, a system interrupt will occur provided the Master Interrupt Enable is set. This is useful for software development and debugging.

IO Enable: When this bit is set to a one, the Wizard chip for the referenced channel is enabled. When this bit is zero, the Wizard chip is disabled.

Pre-emphasis Enable: When this bit is set to a one, the Wizard chip for the referenced channel will provide 20% pre-emphasis of the high-speed serial output signal. When this bit is zero, the pre-emphasis level will be 5%.

Internal Loop-back Enable: When this bit is set to a one, the Wizard chip for the referenced channel is placed in internal loop-back mode. In this mode the transmitted serial data is routed internally directly to the receiver inputs, the serial outputs are held in a high-impedance state. When this bit is zero, the chip operates in normal external mode.

Lock Reference Enable: When this bit is set to a one, the Wizard chip receiver clock for the referenced channel is frequency locked to the transmit clock. This puts the chip in transmit only mode; the receiver parallel outputs are all in a high-impedance state. When this bit is zero, the receiver clock is locked to the received data stream.

PRBS Enable: When this bit is set to a one, the Wizard chip for the referenced channel will transmit a $2^7 - 1$ pseudorandom bit stream on the high-speed serial output and the receiver will check and verify the data pattern. The result will be available on the RKLSB line; a high level indicating a valid pattern. When this bit is zero, the PRBS function is disabled.

TX Enable: When this bit is set to a one, the transmit state-machine for the referenced channel is enabled. When this bit is zero, the transmit state-machine is disabled.

RX Enable: When this bit is set to a one the receive state-machine for the referenced channel is enabled. When this bit is zero, the receive state-machine is disabled.

TX Interrupt Enable: When this bit is set to a one, the transmit interrupt for the referenced channel is enabled. A transmit interrupt can be asserted at the end of each message by setting this bit. When this bit is zero, the transmit interrupt is disabled.

RX Interrupt Enable: When this bit is set to a one, the receive interrupt for the referenced channel is enabled. A receive interrupt can be asserted when a message is received by setting this bit. When this bit is zero, the receive interrupt is disabled.

RX Overflow Interrupt Enable: When this bit is set to a one, the receive FIFO overflow interrupt for the referenced channel is enabled. This will cause an interrupt to occur when an attempt is made to write to a full FIFO. When this bit is zero, the receive FIFO overflow interrupt is disabled.

RX Almost Full Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level is equal or greater to the value specified in the WIZ_CHAN_RX_AFL_LVL register, provided the master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from either the respective channel status register, or the Interrupt Status register.

TX Almost Empty Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level is equal or less than the value specified in the WIZ_CHAN_TX_AMT_LVL register, provided the master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the respective channel status register.

Sync Disable: When this bit is set to a one, the receiver does not wait for the sync pattern to be detected, but starts storing received data to the receive FIFO as soon as the receiver is enabled. This process will continue until the receive FIFO is full or the receiver is disabled. When this bit is zero, the receiver waits until the sync pattern is detected before storing data. Once the sync pattern has been seen, the next 2048 16-bit data words are stored in the receive FIFO.

WIZ_CHAN0/1_STATUS

[0x0014, 0x0044] Status Read / Latch Clear Write

Status Register

Data Bit	Description
31	Interrupt Status
30-15	Spare
19	Read DMA Interrupt Detected
14	Write DMA Interrupt Detected
13	Read DMA Error Detected
12	Write DMA Error Detected
11	Local Interrupt Detected
10	Receive FIFO Overflow Detected
9	Transmit Interrupt Detected
8	Receive Interrupt Detected
7	Spare
6	Transmit FIFO Full
5	Transmit FIFO Almost Empty
4	Transmit FIFO Empty
3	Receive Data Valid
2	Receive FIFO Full
1	Receive FIFO Almost Full
0	Receive FIFO Empty

FIGURE 7 PMC-WIZARD CHANNEL STATUS REGISTER

Receive FIFO Empty: When a one is read, the receive data FIFO for the corresponding channel contains no data; when a zero is read, there is at least one data word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data words in the receive data FIFO for the corresponding channel is greater or equal to the value written to the almost full level register for that channel; when a zero is read, the level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO for the corresponding channel is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive data valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO is empty, because as soon as the first word is written into the FIFO, it is read out to be ready for a PCI read cycle. When this bit is a zero, it indicates that there is no valid receive data remaining.

Transmit FIFO empty: When a one is read, the transmit data FIFO for the corresponding channel contains no data; when a zero is read, there is at least one data word in the FIFO.

Transmit FIFO almost empty: When a one is read, the number of data words in the transmit data FIFO for the corresponding channel is less than or equal to the value written to the almost empty level register for that channel; when a zero is read, the level is more than that value.

Transmit FIFO full: When a one is read, the transmit data FIFO for the corresponding channel is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive interrupt detected: When a one is read, it indicates that a message has been received since the status latch was last cleared. A zero indicates that no message was received since the latch was cleared.

Transmit interrupt detected: When a one is read, it indicates that a. A zero indicates that.

Receive FIFO overflow: When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. A zero indicates that no overflow condition has occurred.

Local interrupt detected: When a one is read, it indicates that an enabled user interrupt condition has occurred. A zero indicates that no enabled user interrupt condition is active.

Write DMA error detected: When a one is read, it indicates that a write DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is a one. A zero indicates that no error has occurred.

Read DMA error detected: When a one is read, it indicates that a read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is a zero. A zero indicates that no error has occurred.

Write DMA interrupt detected: When a one is read, a write DMA interrupt is latched. This indicates that the scatter-gather list for the current write DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no write DMA interrupt is pending.

Read DMA interrupt detected: When a one is read, it indicates that a read DMA interrupt is latched. This indicates that the scatter-gather list for the current read DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no read DMA interrupt is pending.

Interrupt status: When a one is read, an enabled channel interrupt condition is active and a system interrupt should be asserted. A zero indicates that no enabled channel interrupt is active.

WIZ_CHAN0/1_WR/RD_DMA_PNTR

[0x0018, 0x001C, 0x0048, 0x004C] DMA Address Register (Write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 8 PMC-WIZARD CHANNEL DMA POINTER REGISTER

These write-only ports are used to initiate a scatter-gather DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until a bit in one of the next pointer values read indicates that it is the end of the chain.

WIZ_CHAN0/1_FIFO

[0x0020, 0x0050] Write TX/Read RX FIFO Port

TX / RX FIFO Port	
Data Bit	**Description**
31-0	FIFO Data 31-0

FIGURE 9 PMC-WIZARD CHANNEL FIFO PORT

These ports are used to make single-word accesses to the channel data FIFOs.

WIZ_CHAN0/1_RX_AFL_LVL

[0x0024, 0x0054] RX Almost Full Level Register (read/write)

RX Almost Full Level Register

Data Bit	Description
31-16	Spare
15-0	RX FIFO almost full level

FIGURE 10 PMC-WIZARD CHANNEL RX ALMOST FULL LEVEL REGISTER

These read/write ports access the receiver almost-full level registers for the respective channels. When the number of data words in the receive data FIFO is equal or greater than this value, the almost full status bit is set and an interrupt may be generated if it is enabled.

WIZ_CHAN0/1_TX_AMT_LVL

[0x0028, 0x0058] TX Almost Empty Level Register (read/write)

TX Almost Empty Level Register

Data Bit	Description
31-16	Spare
15-0	TX FIFO almost empty level

FIGURE 11 PMC-WIZARD CHANNEL TX ALMOST EMPTY LEVEL REGISTER

These read/write registers access the transmitter almost-empty level registers for the respective channels. When the number of data words in the transmit data FIFO is equal or less than this value, the almost empty status bit is set and an interrupt may be generated if it is enabled.

WIZ_CHAN0/1_TX/RX_FIFO_COUNT

[0x002C, 0x005C] TX/RX FIFO Data Count Port (read only)

FIFO Data Count	
Data Bit	**Description**
31-12	Spare
11-0	FIFO Data Words Stored

FIGURE 12 PMC-WIZARD CHANNEL TX/RX FIFO DATA COUNT PORT

These read-only ports report the number of 32-bit data words in the corresponding transmit/receive FIFO. When data is loaded into the receive data FIFO, the first four words will be immediately read and held in a pipeline in preparation for a read DMA. Starting with the rev. B firmware, data words in the receive-data pipeline are included in the count. This makes the maximum count of the receive FIFO 0x1003 rather than 0xFFF. The maximum transmit data count is still 0xFFF.

WIZ_CHAN0/1_SYNC_PATTERN

[0x0034, 0x0064] Sync Pattern Register (read/write)

Sync Pattern Register	
Data Bit	**Description**
31-0	Sync Pattern

FIGURE 13 PMC-WIZARD CHANNEL SYNC PATTERN REGISTER

These read/write registers hold the pattern that the receive state-machines looks for to indicate the beginning of a message. When this pattern is recognized, the following 2048 16-bit words will be stored in the receive FIFO. Starting with the rev. B firmware, a control bit has been added to the channel control register to disable detection of the sync pattern before data is stored in the receive FIFO.

WIZ_CHAN0/1_IDLE_CONFIG

[0x0038, 0x0068] Idle Configuration Register (read/write)

Idle Configuration Register	
Data Bit	**Description**
31-16	Idle Count
15-0	Idle Pattern

FIGURE 14 PMC-WIZARD CHANNEL IDLE CONFIGURATION REGISTER

These read/write registers hold the idle configuration that the transmit state-machines inserts between messages. The lower 16 bits are the data pattern to be inserted and the upper 16 bits are the count that specifies how many times the idle pattern will be inserted (minimum of two idle patterns).

Loop-back

The Engineering kit has reference software, which includes a channel-to-channel loop-back test. The MDM-9-pin connectors for the two Wizard channels are connected with a cable consisting of four twisted pairs. The twisted pairs should have a minimum of 4 twists per inch to insure signal integrity.

The test requires the following pins connected.

Signal	P1 Pin	P2 Pin	Signal
DINARX+	5	6	DOUTBTX+
DINARX-	9	1	DOUTBTX-
DOUTATX+	6	5	DINBRX+
DOUTATX-	1	9	DINBRX-

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-Wizard. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3# 25	26	
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0# 51	52	
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 15 PMC-WIZARD PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-Wizard. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2# 31		32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1# GND	43		44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 16 PMC-WIZARD PN2 INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-Wizard. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-Wizard is constructed out of 0.062-inch thick FR4 material.

Surface-mount components are used. The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-Wizard design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 Fax
support@dyneng.com

Specifications

Host Interface:	PCI Mezzanine Card
Serial Interfaces:	Two Wizard channels
Transfer rate:	80 MHz x 16-bit ->1.6 Gbit serial for each Wizard channel.
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	Each channel has an interrupt for TX almost empty, Rx almost full, Read and write DMA interrupts are also implemented
DMA:	Scatter/Gather DMA Support implemented
Onboard Options:	All Options are Software Programmable
Interface Options:	Two 9-pin MDM connectors for channel 0, 1.
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Through-Hole and Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC-Wizard	http://www.dyneng.com/pmc_Wizard.html Standard version with two 4KB FIFOs per channel, standard Wizard timing and protocol.
PMC-Wizard-Eng-1	Engineering Kit for the PMC-Wizard board-level schematics (PDF) and MDMCable9
PMC-Wizard-Eng-2	Board-level schematics [PDF], Software Driver and sample application, and MDMCable9
MDMCable9	9-pin MDM connectors (2) - four shielded twisted pairs