

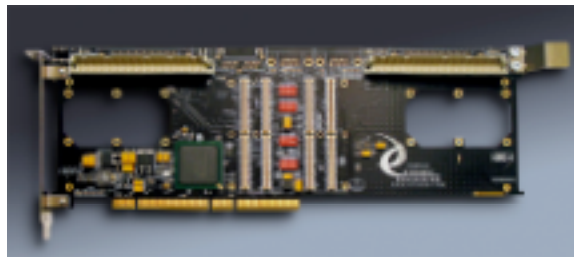
DYNAMIC ENGINEERING

150 Dubois St. STE 3, Santa Cruz, Ca 95060
831-457-8891 **Fax** 831-457-4793
<http://www.dyneng.com>
sales@dyneng.com
Est. 1988

User Manual

PCIBPMCx2

PCI 2 Slot PMC Compatible Carrier



Revision A4
Corresponding Hardware: Revision C/D
Fab number 10-2005-0303/4

PCIBPMCx2
PCI and PMC Compatible Carrier

Dynamic Engineering
150 Dubois St. STE 3
Santa Cruz, CA 95060
831457-8891
831457-4793 FAX

©2005-2007 by Dynamic Engineering.
Other trademarks and registered trademarks are owned by their
respective manufactures.
Manual Revision A4 Revised 10/15/07

This document contains information of proprietary interest to Dynamic Engineering. It has been supplied in confidence and the recipient, by accepting this material, agrees that the subject matter will not be copied or reproduced, in whole or in part, nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.



Table of Contents

PRODUCT DESCRIPTION	5
Shunt Settings	6
DipSwitch Settings	7
Reserved Pins Routing	11
Options	11
PMC Module Backplane IO Interface Pin Assignment	14
PMC Module Pn4 Ethernet and Serial Pin Assignment	15
APPLICATIONS GUIDE	16
Interfacing	16
Construction and Reliability	17
Thermal Considerations	17
WARRANTY AND REPAIR	18
Service Policy	18
Out of Warranty Repairs	18
For Service Contact:	18
SPECIFICATIONS	19
ORDER INFORMATION	20



List of Figures

FIGURE 1	PCIBPMCX2 SLOT0 INTERRUPTS SCHEMATIC	9
FIGURE 2	PCIBPMCX2 SLOT1 INTERRUPTS SCHEMATIC	10
FIGURE 3	PCIBPMCX2 PN4 INTERFACE STANDARD	14
FIGURE 4	PCIBPMCX2 PN4 ETHERNET , SERIAL	15

Product Description

PCIBPMCx2 is part of the Dynamic Engineering PCI and PMC Compatible family of modular I/O components. The PCIBPMC adapts 2 PMCs to one PCI slot.

Embedded applications frequently require real time processing coupled with special purpose IO. With the PCIBPMCx2's two slots; a PrPMC can be matched with another PMC to make a high bandwidth processing node. The PrPMC can communicate with the host for set-up, and then use the local bus to control and transfer data with the special purpose IO card. For example the PMC-BiSerial-III-HW1 provides 32 channels of Manchester encoded IO, and when matched with a PrPMC can control or monitor a large system in real time.

The PCIBPMCx2 has programmable [switch] options for interrupts, and other features to customize for your application.

Special features:

- Universal PCI voltage
- PCI, PCI-X compatible
- Device Hiding and Opaque Memory options
- LED on PMC Busmode "Present" for each slot.
- LED's on plus 12V, minus 12V, plus 5V, plus 3.3V, and VIO
- 8A regulator for PMC 3.3V supply
- Selection switch for PCI3.3 or regulated 3.3
- Selectable secondary VIO.
- 32 or 64 bit operation on either bus
- 133, 100, 66 or 33 MHz operation.
- Front panel connector access through PCI bracket
- User IO [Pn4] available through one of two cable connectors (DIN IDC or SCSI II compatible) Spare pins on SCSI connector can be shunt selected to power or ground.
- Cooling cutout for increased airflow to PMCs
- Optional Fan(s) to increased airflow
- Optional Ethernet connectors to support PMCs with Ethernet
- Optional Serial Port connectors to support PMCs with Serial Ports
- JTAG programming support

The PCIBPMCx2 is ready to use with the default settings. Just install the PMC onto the PCIBPMC and then into the system. There are a few settings that can optimize performance.



Shunt Settings

Please note that the settings affect both PMC slots.

Select the appropriate VIO for your PMC(s). A PMC can be 3.3V or 5V or “universal”. Please select the 3.3 or 5V VIO choice with the shunt **J4**. The Voltage choices are marked. Install the shunt for 3.3V operation; open for 5V operation.

The VIO plane is a reference for the IO level. The specification does not prohibit larger current consumption from these pins. The PCIBPMC design utilizes a MOSFET to control the 5V or 3.3V rails onto the VIO plane. Max consumption on the VIO rail is 3A. The maximum power draw of a PMC is 7.5W leaving a large safety factor. [The factory setting is 3.3V on the secondary VIO rail.](#)

Select the 3.3V source for your PMC. Some backplanes have 3.3 and some do not. Sometimes the isolation provided by an inline power supply is useful. Sometimes there is not enough 3.3V to supply all of the devices and it is handy to convert some of the 5V rail to 3.3V. The PCIBPMCx2 has a switching DC/DC power converter built in.

When shunt **J1** is installed the switching regulator is enabled and the backplane power path is disabled. The switching regulator controls a low impedance MOSFET to pass the 5V onto the 3.3V rail. When the switching regulator senses that the voltage is within tolerance the MOSFET is disabled. When the voltage falls below the threshold the MOSFET is enabled. An inductor and several large value tantalum capacitors are used to provide “clean” power to the PMCs. The switching regulator is much more efficient than a linear regulator resulting in lower heat dissipation and a higher MTBF. When shunt J1 is **not** installed, the 3.3V rail from the backplane is routed to the PMC. [The factory setting is installed.](#)



DipSwitch Settings

Please note that the switch numbering and '1' and '0' definitions are per the silk screen.

The dipswitches are numbered SW4, SW3, SW1, SW2 from top to bottom and are located between the PMC connectors. SW3,4 are used to control the PMC interrupt routing. SW2 is used for the GPIO port. SW1 controls the Bridge operation. SW 3,4 are oriented with pin 1 to the right and SW1,2 are positioned with pin 1 on the left [see “dot” in silkscreen]. The “on” position is the closed position for the switch.

Switch 1: Special selections for the 31154 Bridge

For more information please refer to the Intel® documentation

Position 1 corresponds to S_MAX100. When closed the signal is '0'. When open the signal is '1'. When set to '1' the secondary [PMC] side is limited to 100 Mhz in PCI-X mode. [The factory setting is '0'.](#)

Position 2 corresponds to S_PCIXCAP. When closed the signal is '0'. When open the signal is '1'. When set to '1' PCI-X operation is enabled for the secondary side. [The factory setting is '0'.](#)

Position 3 corresponds to OPAQUE_EN. When closed the signal is '0'. When open the signal is '1'. When set to '1' Opaque Memory is enabled to establish the Base and limit registers used to create a private memory space. [The factory setting is '0'.](#)

Position 4 corresponds to IDSEL_MASK. When closed the signal is '0'. When open the signal is '1'. When set to '1' hide the devices attached to the PMC slots from the host after reset. [The factory setting is '0'.](#)

Position 5 corresponds to DEV_64BIT#. When closed the signal is '0'. When open the signal is '1'. When set to '1' 64 bit operation is enabled for the PMC slots. [The factory setting is '0'.](#)

Position 6 is connected to the Monarch pin for slot 0. When open a 4.7K pull-up to VIO is used to control the Monarch signal [Pn2-64]. When closed the Monarch signal is set to gnd. [The factory setting is '1'.](#)



Position 7 corresponds to S_M66EN. When closed the signal is '0'. When open the signal is '1' assuming that the PMC's do not pull the signal down. SM66EN acts as an open drain signal with any of the nodes capable of reducing the clock rate and all nodes required to operate at the higher rate. Select the secondary side [PMC] PCI bus frequency. The options are to use the PCI bus speed [primary] or to force 33 MHz on the secondary side. The PMC to be installed must be 66 MHz compliant to use the 66 MHz secondary side option. '1' = 66 MHz capable secondary side. '0' = 33 MHz. Please note that PCI-XCAP will override if set to enabled. [The factory setting is '1'](#).

The SM66EN signal is also routed to the PMC connector pin M66EN. If the PMC uses the M66EN as an input then the dipswitch can be used to control the frequency. If the PMC uses the M66EN pin as a control, then the Switch may have no effect. For example if the switch is in the '1' position and the PMC is selecting M66EN = '0' then the PMC will "win" and the signal will be at the 33 MHz setting. Both the dipswitch and the PMC M66EN have to be enabled for 66 MHz operations.

Position 8 corresponds to P_M66EN. When closed the signal is '0'. When open the signal is '1'. Select '1' to use the PCI bus speed and '0' to force 33 MHz operation. If the rest of the cards installed on the same PCI segment, and the segment itself are 66 MHz capable then the PCI primary speed will be 66 MHz. If any device on the segment is set to 33 MHz only then the entire segment will operate at 33 MHz. We recommend enabling the 66 MHz operations, and using the bridge to switch to 33 MHz for the PMC. [The factory setting is '1'](#).

Switch 2: GPIO

The 8 switch positions can be read in from the bridge via the configuration space registers. The switch bits 8-1 correspond to the GPIO bits 7-0. The bits can be used for any purpose – Card numbering etc. The GPIO bits are also connected to a test point strip. If the GPIO bits are to be used as outputs be sure that the corresponding switch is in the open position. [The factory setting is open.](#)



Interrupts from the PMC are connected from the PMC to the primary PCI bus. INTA through INTD are mapped indirectly to the primary bus segment.

Switch 3: PMC 0 Interrupt routing control

The PMC INTA-D signals are tied to switch positions 4-1 and 8-5. The upper bits are tied to Switch 4[8-5] and form the slot 0 connection to the Interrupt Intermediate bus. The lower bits are tied to the PCI connector interrupts. The right hand side connections in the schematic are tied to the PMC Slot 0 interrupts.

Most PMC cards will have only one interrupt and present that on INTA. With switch 4 closed the interrupt from PMC 0 is connected to INTA on the PCI [primary bus].

If Slot 0 is not occupied or does not use interrupts; the interrupt from Slot 1 will need to be routed to INTA on the PCI bus.

The factory setting is switch 4 closed and the rest open.

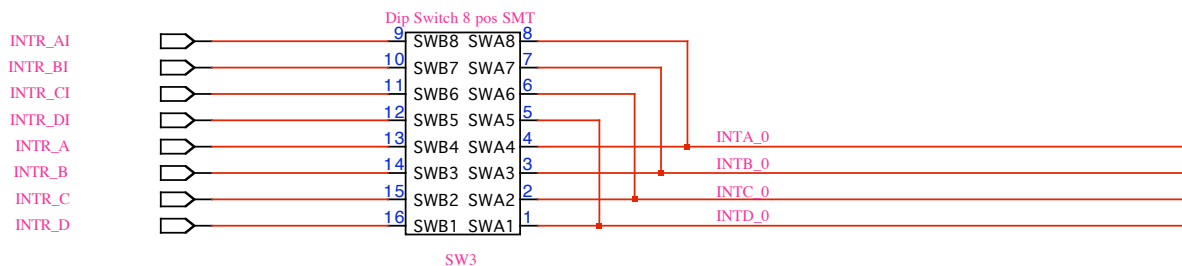


FIGURE 1 PCIBPMCX2 SLOT0 INTERRUPTS SCHEMATIC

Switch 4: PMC 1 Interrupt routing control

The PMC INTA-D signals are rotated and tied to switch positions 4-1 and 8-5. INTA is on pins 8 and 3, INTB is on 7 and 2 and so forth. The upper bits are tied to Switch 3 and form the second connection on the Interrupt Intermediate bus. The lower bits are tied to the PCI connector for direct connection to the PCI Interrupts. The right hand side connections in the schematic are tied to the PMC Slot 1 interrupts.

Most PMC cards will have only one interrupt and present that on INTA. With switch 3 closed the interrupt from PMC 1 is connected to INTB on the PCI [primary bus]. With two PMC's installed and PMC 0 using interrupts this is the correct configuration. Slot 0 on INTA and Slot 1 on INTB.

With switch 8 closed on SW3 and SW4 the intermediate bus ties INTA to INTA between the PMC sites. If Slot 0 is not in use or not using INTA then PMC 1 can be routed through to the PCI interrupt INTA by closing switch 4 on SW3.

The factory setting is switch 3 closed and the rest open.

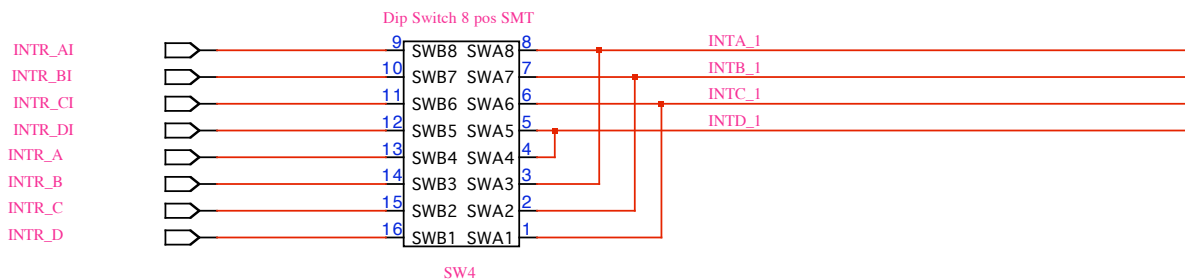


FIGURE 2 PCIBPMCX2 SLOT1 INTERRUPTS SCHEMATIC

Please note that SW3 and SW4 are installed with pin one on the RHS when viewing the card with the PCI fingers down. SW3 DIP switch number 1 is on the RHS and DIP switch number 8 is on the LHS. For a “mental picture” you can rotate the schematic counter-clockwise 90 degree’s. With the switch in the up position the switch is open. With the individual switches in the down position the switches are closed [making the connection].

To implement the INTA from slot 1 to INTA on the PCI bus example: Starting with the right hand side of SW3 the first three switches would be up, and the 4th down, then the next three up and the 8th down to correspond to SW3 switch 4 and 8 closed. On SW4 the first 7 switches would be up and the last [8th] down.

The IDSEL is AD16 for slot 0 and AD17 is used for slot 1 [secondary PCI]. Fab Rev 1-3 The IDSEL is selectable to be AD20 for slot 0 and AD21 is used for slot 1 or AD16 and Ad17 respectively. Shunt J16 when installed provides AD16, AD17 and open selects AD20, AD21. Rev 4+

The PCI reserved signals are routed to the PMC reserved pins in accordance with the PMC specification to allow for future signal definitions or special user signaling.

Reserved Pins Routing

<u>PCI</u>	<u>PMC</u>
A9	Pn2-8
B10	Pn2-9
A11	Pn2-10
B14	Pn1-10
A40	Pn1-41
A41	Pn1-42
B63	Pn3-1
A92	Pn3-59
B92	Pn3-63
B93	Pn3-61
A94	Pn3-64

In Addition Jn2 pins 58 and 64 are pull-ed up to VCC_IO with 4.7KΩ. Pin 60 is open. This configuration works with most Monarch capable PMCs. Please contact Dynamic Engineering if you need alternate settings.

Options

Dynamic Engineering offers multiple versions of the PCIBPMCx2 design.

In addition to the basic bridged version there are options for Ethernet, Fan, Serial ports, and minimization.

The PCIBPMCx2 features cooling cutouts designed to support the addition of a fan in one of two positions for each PMC. On PrPMC's and other PMCs with high thermal loads the fan option is a good idea. On cards with a lower thermal profile the fan is not needed. The fan produces 8 CFM in a small area to create a high LFM rating suitable for most cooling requirements. The fan used has a relatively low noise rating for quiet



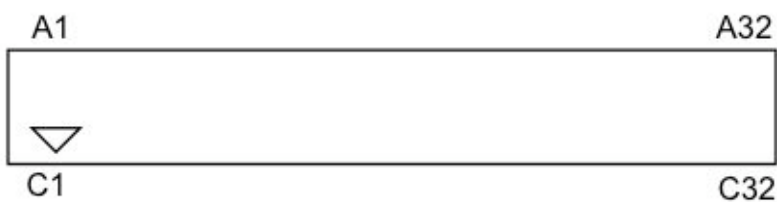
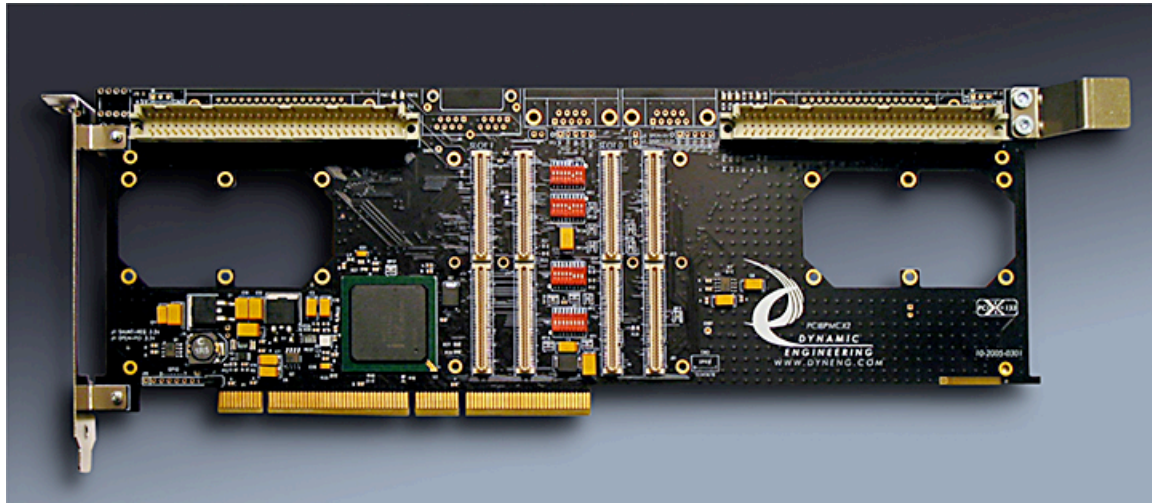
operation. Position 1 is closest to the PCI bezel and position 2 is closer to the PMC connectors. For position 3 and position 4 locations continue counting left to right.

Some PMCs support Ethernet connections over the Pn4 connector with pins specified by the PICMG standard 2.15. PCIBPMCx2 supports Ethernet capable cards with an optional two-position RJ45 connector on the top edge of the card. Slot 0 has this option.

Some PMCs support serial channels on Pn4 with pins specified by PICMG standard 2.15. PCIBPMCx2 supports serial capable cards with an optional pair of DB9F connectors on the top edge of the card. Slot 0 has this option.

In addition the PCIBPMC has two options for Pn4 signal routing. VME style 2x32 pin header [shown] or a SCSI style connector.

Please mix and match options, as you need them.



The “VME” connectors are oriented as shown in the picture and the diagram. Pin C1 is the lower left corner pin. Pin C1 corresponds to the cable wire number 1 for a standard header inserted into the connector on the PCIBPMCX2. The mating part number is 120-964-455 Panduit, DIN-IDCA-64CSB-TG30 Robinson Nugent, Berg also has a part which is slightly taller.

Cables and breakouts are available from Dynamic Engineering – Please see DINterm64 and DINribn64 products from the Dynamic Engineering website.



PMC Module Backplane IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface – from Pn4 to the PCIBPMCx2 connectors. Also see the User Manual for your PMC board for more information. Please note that P2 or P3, P4 or P5 are installed not both.

DIN IDC [P3,P5]		SCSI II [P2,P4]		Pn4	
C1	A1	1	35	1	2
C2	A2	2	36	3	4
C3	A3	3	37	5	6
C4	A4	4	38	7	8
C5	A5	5	39	9	10
C6	A6	6	40	11	12
C7	A7	7	41	13	14
C8	A8	8	42	15	16
C9	A9	9	43	17	18
C10	A10	10	44	19	20
C11	A11	11	45	21	22
C12	A12	12	46	23	24
C13	A13	13	47	25	26
C14	A14	14	48	27	28
C15	A15	15	49	29	30
C16	A16	16	50	31	32
C17	A17	17	51	33	34
C18	A18	18	52	35	36
C19	A19	19	53	37	38
C20	A20	20	54	39	40
C21	A21	21	55	41	42
C22	A22	22	56	43	44
C23	A23	23	57	45	46
C24	A24	24	58	47	48
C25	A25	25	59	49	50
C26	A26	26	60	51	52
C27	A27	27	61	53	54
C28	A28	28	62	55	56
C29	A29	29	63	57	58
C30	A30	30	64	59	60
C31	A31	31	65	61	62
C32	A32	32	66	63	64
		33	67	Open, +5 or GND via J2 silk screen defined	
		34	68	Open, +5 or GND via J3	

FIGURE 3

PCIBPMCx2 PN4 INTERFACE STANDARD

Read table:

P3-C1 = P2-1 = Pn4-1

P3-A1 = P2-35 = Pn4-2

etc.



PMC Module Pn4 Ethernet and Serial Pin Assignment

Ethernet[J6]		Serial[J7,J8]	Pn4 Slot 0	
11	14		1	2
12	15		3	4
			5	6
13	17		7	8
16	18		9	10
			11	12
21	24		13	14
22	25		15	16
			17	18
23	27		19	20
26	28		21	22
			23	24
			25	26
		13	27	28
		23	29	30
			31	32
		12	33	34
		22	35	36
			37	38
			39	40
			41	42
			43	44
			45	46
			47	48
			49	50
			51	52
			53	54
			55	56
			57	58
			59	60
			61	62
			63	64

FIGURE 4

PCIBPMCX2 PN4 ETHERNET , SERIAL

The channel number is shown then the pin number. For example On the ethernet connector J6, there are two RJ45 connectors. Port 1 pin 1 is tied to Pn4 pin 1, Port 2 pin 8 is tied to pin 22 of Pn4. When the Ethernet and Serial options are installed the corresponding pins on Pn4 are no longer connected to the SCSI or VME connectors. The unaffected pins are still connected.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation

The PMC is mounted to the PCIBPMCx2 prior to installation within the chassis. For best results: with the PCI bracket installed, install the PMC at an angle so that the PMC front panel bezel penetrates the PCI bracket then rotate down to mate with the PMC [PnX] connectors. The rear slot does not have the bezel interaction and can be mounted directly.

There are four mounting locations per PMC. Two into the PMC mounting bezel, and two for the standoffs near the PMC bus connectors.

Start-up

Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId for the PMC installed and an interrupt level. If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCIBPMCx2 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the PMCs installed onto the PCIBPMCx2 than the PCIBPMCx2 itself, and it is smart system design when it can be achieved.



Construction and Reliability

The PCIBPMCx2 is constructed out of 0.062 inch thick FR4 material. Cooling cutouts have been designed into the product for improved air flow to the PMC sites. The components on the PCIBPMCx2 are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in the situation where a large portion of the board has little or no power dissipation.

A fan option is available for high thermal load PMCs or for a chassis with a lack of air circulation.

Surface mounted components are used. The connectors are SMT for the PMC bus and through hole for the IO.

The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC Module is secured against the carrier with the PMC connectors. It is recommended, for enhanced security against vibration, that the PMC mounting screws are installed. The screws are supplied with the PMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels and other PMC hardware available at a reasonable cost if your PMC was not shipped with some of the required attachment hardware or if it has been misplaced.

Thermal Considerations

If the PMC installed has a large heat dissipation; forced air cooling is recommended.



Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

<http://www.dyneng.com/warranty.html>

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is \$100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite 3
Santa Cruz, CA 95060
831-457-8891 831-457-4793 fax InterNet Address support@dyneng.com



Specifications

Logic Interfaces:	PCI, PCI-X Interface 33/32 <--> 133/64
Access types:	PCI bus accesses
CLK rates supported:	133, 100, 66, 33 MHz PCI clock rates
Software Interface:	transparent Bridge. 31154 registers in configuration space
Initialization:	switch selections for VIO, 3.3V source, primary and secondary clock rates, special bridge based features and cable options
Interface:	PMC front bezel via PCI bracket and User IO connector via DIN ribbon and or SCSI II connector
Dimensions:	full length PCI board with offset PCI card guide support.
Construction:	High Temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.



Order Information

standard temperature range 0-70°C

PCIBPMCx2

full length PCI card with 2 PMC positions

-FAN(1,2,3,4,13,14,23,24) [fan installed in position 1 or 2 or 3 or 4 or 1 and 3 or 1 and 4 or 2 and 3 or 2 and 4]

-SER [serial ports installed]

-ENET [ethernet connectors installed]

-ROHS [ROHS compliant parts and process]

<http://www.dyneng.com/pcibpmcx2.html>

HDEterm68

<http://www.dyneng.com/HDEterm68.html>

68 pin SCSI II to 68 screw terminal converter with DIN rail mounting.

HDEcabl68

<http://www.dyneng.com/HDEcabl68.html>

SCSI cables with latch blocks or thumbscrews and various lengths are available. Custom lengths can be ordered.

DINterm64

<http://www.dyneng.com/DINterm64.html>

64 pin ribbon cable to to 64 screw terminal converter with DIN rail mounting.

DINribn64

<http://www.dyneng.com/DINribn64.html>

64 pin ribbon cable with strain relief. Add -XX for number of inches. 36" is default.

All information provided is Copyright Dynamic Engineering

