PCI LVDS 8R

8 Channel LVDS Serial Interface

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This product has been designed to operate with PCI and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Introduction

The PCI_LVDS_8R features 8 channels of LVDS input. Each input channel is composed of 3 serial data pairs plus a reference clock. The reference clock can operate at speeds up to 175 MHz. The National DS90CR218 [TIA/EIA-644] or equivalent receiver chip is used. The receiver converts the three parallel streams into 21 bit parallel data. The PCI_LVDS_8R implements the lower two serial streams for a 14 bit parallel interface. The upper serial stream and corresponding upper 7 bits are defined and routed to allow for future expansion and alternate protocols to be implemented.

The LVDS channels are grouped two per Front End [FE] Xilinx. The FE Xilinx receives the data and performs data filtering to allow programmed patterns to start capture and other patterns to be stored. The Data width is built up from 14 to 16 bits with the addition of parity. The data samples are combined to form 32 bit words before being written to the Input FIFO. There is one Input FIFO per LVDS channel. 1K x 32.

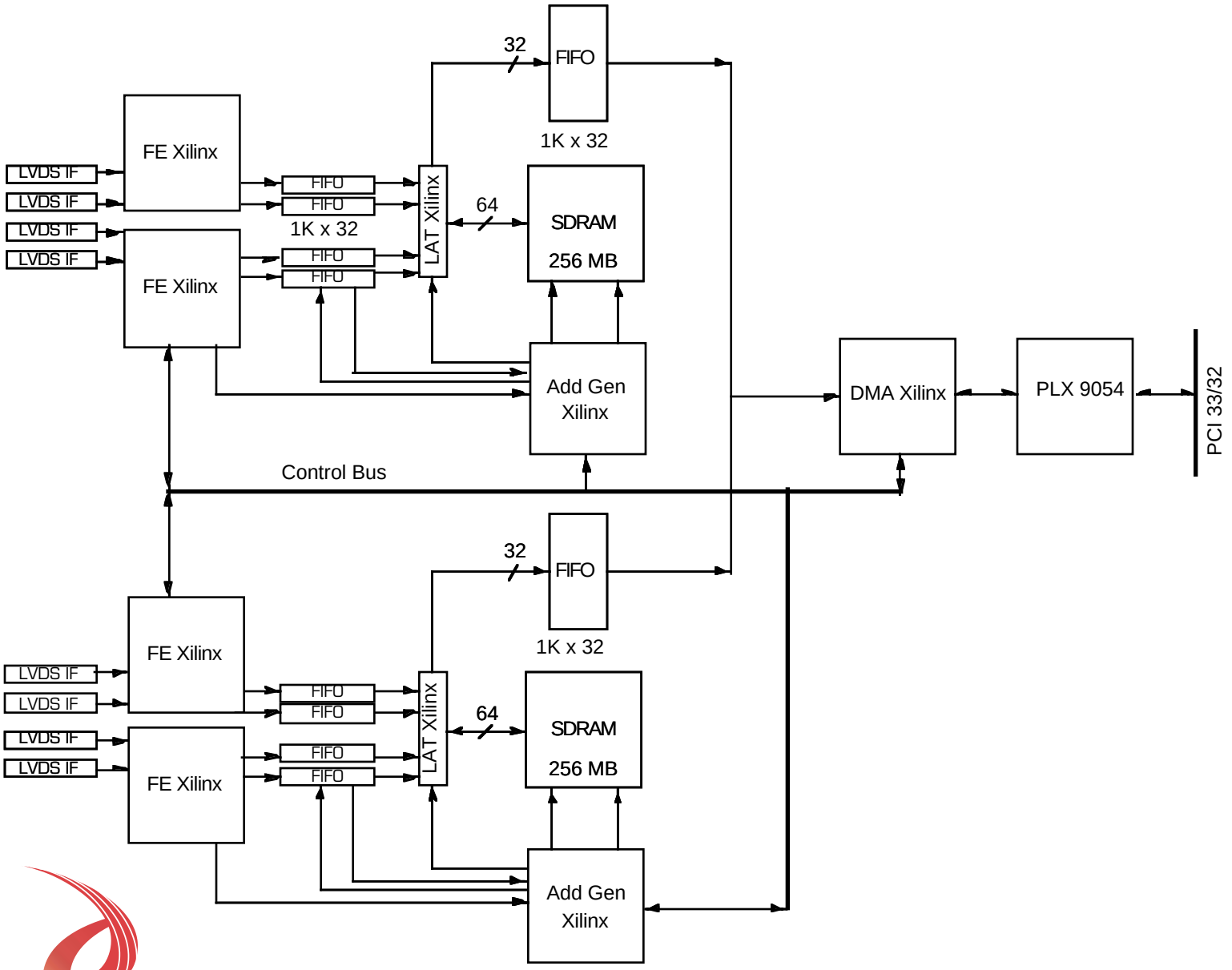
One Latch Xilinx handles 4 LVDS channels – the output from two FE Xilinx. The data is read from the Input FIFO by the Latch Xilinx and either written to the SDRAM or to the Output FIFO. The data is read into the Latch Xilinx at 66 MHz and written to the SDRAM at 33 MHz. The data width is doubled from 32 bits to 64 bits in this path. The Data can also be read from the SDRAM and written to the Output FIFO. When data is written to the Output FIFO the width is 32 bits and the rate is 66 MHz. The Address Generator controls the Latch Xilinx and the SDRAM. The data from the output FIFO can be read directly or as a DMA stream.

The Address Generator is used to control the Latch Xilinx [data path], and provide the address control for the SDRAM. After Power-Up the Address Generator provides the control words to the SDRAM to initialize operation and then the proper control sequences for refresh and burst access. In Capture mode the Address Generator polls the Input FIFOs for data to be transferred into the SDRAM. When a FIFO's Half-Full flag is set, data is transferred from the FIFO through the Latch Xilinx into the SDRAM. In Retrieve mode the data is read from the SDRAM and loaded into the Output FIFO. The Output FIFO is polled to see if there is room for the next burst of data. In Direct mode the data is moved from the Input FIFO through the Latch Xilinx to the Output FIFO without using the SDRAM.

The Data in the Output FIFO passes through the DMA Xilinx before the PLX [PCI interface] has access. The data is written into the Output FIFO at 66 MHz and read out at 33 Mhz. The interface supports DMA and target reads. The 2:1 load to read bandwidth insures rapid and efficient data transfer in Retrieve mode.

The FE design includes a software write path and load register to allow the software to load data words into the Input FIFO directly. The FE design also has a 12 bit counter that can be used to load data automatically into the FIFO for performance testing. The Counter inserts data at 33MHz. into the data path to provide a continuous data stream. The counter can be used to cause Direct or Capture mode operations. Retrieve can be used after capture to read the data back for test and development purposes.

The hardware as of this revision has all Channels and all data paths tested. An 8 channel LVDS data simulator was used with multiple patterns, speeds, and programming scenarios to check on all modes of operation.


32
FIFO
1K x 32
FE Xilinx
LVDS IF
LVDS IF
LVDS IF
LVDS IF
FIFO
FIFO
1K x 32
FIFO
FIFO
LAT Xilinx
64
SDRAM
256 MB
FE Xilinx
Add Gen
Xilinx
DMA Xilinx
PLX 9054
PCI 33/32
Control Bus
32
FIFO
1K x 32
FE Xilinx
LVDS IF
LVDS IF
LVDS IF
LVDS IF
FIFO
FIFO
FIFO
FIFO
LAT Xilinx
64
SDRAM
256 MB
FE Xilinx
Add Gen
Xilinx

Memory Map

(Addresses shown as byte)
Addresses are offsets from the PCI Base Address defined by the system and the PLX 9054. The PLX 9054 requests several BARs. The BAR associated with Space 0 is the base address for the internal PCI_LVDS_8R hardware. The CardId = 9054. The VendorId = 10B5. The Local Space must be enabled by writing a 0x0001 to Space_0_Base [PLX 9054 internal register]. The Interrupt must be enabled within the PLX for the interrupts described within this document to reach the host. Please download the PLX 9054 manual for complete details.

Front End Filter Channels 0,1

Decode number	Address offset	Chip	Definition
0	0000	FE01	TAG_DEF_0
	0004	FE01	X0_STOP
	0008	FE01	X1_STOP
	000C	FE01	Y0_STOP
	0010	FE01	Y1_STOP
	0014	FE01	Z0_STOP
	0018	FE01	Z1_STOP
	001C	FE01	X_TOTAL_0_RDBK
	0020	FE01	X_TOTAL_1_RDBK
	0024	FE01	0,1_DTA_PAT
	0028	FE01	FIFO_0 WRT
	002C	FE01	FIFO_1 WRT
	0030	FE01	TAG_DEF_1
	0034	FE01	FE_DONE_0
	0038	FE01	FE_DONE_1
	003C	FE01	Preload data counter 0-1

Front End Filter Channels 2,3

Decode number	Address offset	Chip	Definition
1	0040	FE23	TAG_DEF_2
	0044	FE23	X2_STOP
	0048	FE23	X3_STOP
	004C	FE23	Y2_STOP
	0050	FE23	Y3_STOP
	0054	FE23	Z2_STOP
	0058	FE23	Z3_STOP
	005C	FE23	X_TOTAL_2_RDBK
	0060	FE23	X_TOTAL_3_RDBK
	0064	FE23	2,3_DTA_PAT
	0068	FE23	FIFO_2 WRT
	006C	FE23	FIFO_3 WRT
	0070	FE23	TAG_DEF_3
	0074	FE23	FE_DONE_2
	0078	FE23	FE_DONE_3
	007C	FE23	Preload data counter 2-3

Address Generator Channels 0-3

Decode number	Address offset	Chip	Definition
2	0080	ADDO_3	Start ADD CH 0
	0084	ADDO_3	Start ADD CH 1
	0088	ADDO_3	Start ADD CH 2
	008C	ADDO_3	Start ADD CH 3
	0090	ADDO_3	Length CH 0
	0094	ADDO_3	Length CH 1
	0098	ADDO_3	Length CH 2
	009C	ADDO_3	Length CH 3
	00A0	ADDO_3	CNTL CH 0
	00A4	ADDO_3	CNTL CH 1
	00A8	ADDO_3	CNTL CH 2
	00AC	ADDO_3	CNTL CH 3
	00B0	ADDO_3	SDRAM Base 0-3
	00B4-00B8	ADDO_3	Spare
	00BC	ADDO_3	Status 0-3
3		spare	

Front End Filter Channels 4,5

Decode number	Address offset	Chip	Definition
4	0100	FE45	TAG_DEF_4
	0104	FE45	X4_STOP
	0108	FE45	X5_STOP
	010C	FE45	Y4_STOP
	0110	FE45	Y5_STOP
	0114	FE45	Z4_STOP
	0118	FE45	Z5_STOP
	011C	FE45	X_TOTAL_4_RDBK
	0120	FE45	X_TOTAL_5_RDBK
	0124	FE45	4,5_DTA_PAT
	0128	FE45	FIFO_4 WRT
	012C	FE45	FIFO_5 WRT
	0130	FE45	TAG_DEF_5
	0134	FE45	FE_DONE_4
	0138	FE45	FE_DONE_5
	013C	FE45	Preload data counter 4-5

Front End Filter Channels 6,7

Decode number	Address offset	Chip	Definition
5	0140	FE67	TAG_DEF_6
	0144	FE67	X6_STOP
	0148	FE67	X7_STOP
	014C	FE67	Y6_STOP
	0150	FE67	Y7_STOP
	0154	FE67	Z6_STOP
	0158	FE67	Z7_STOP
	015C	FE67	X_TOTAL_6_RDBK
	0160	FE67	X_TOTAL_7_RDBK

	0164	FE67	6,7_DTA_PAT
	0168	FE67	FIFO_6 WRT
	016C	FE67	FIFO_7 WRT
	0170	FE67	TAG_DEF_7
	0174	FE67	FE_DONE_6
	0178	FE67	FE_DONE_7
	017C	FE67	Preload data counter 6-7

Address Generator Channels 4-7

Decode number	**Address offset**	**Chip**	**Definition**
6	0180	ADD4_7	Start ADD CH 4
	0184	ADD4_7	Start ADD CH 5
	0188	ADD4_7	Start ADD CH 6
	018C	ADD4_7	Start ADD CH 7
	0190	ADD4_7	Length CH 4
	0194	ADD4_7	Length CH 5
	0198	ADD4_7	Length CH 6
	019C	ADD4_7	Length CH 7
	01A0	ADD4_7	CNTL CH 4
	01A4	ADD4_7	CNTL CH 5
	01A8	ADD4_7	CNTL CH 6
	01AC	ADD4_7	CNTL CH 7
	01B0	ADD4_7	SDRAM Base 4-7
	01B4-01B8	ADD4_7	Spare
	01BC	ADD4_7	Status 4-7
7..F		spare	

PLX Interface, Decode and Control

Decode number	Address offset	Chip	Definition
10	0400	DMA Base Control r-w	
	0404		
	0408		
	040C		
	0410		
	0414		
	0418		
	041C		
	0420		
	0424		
	0428		
	042C		
	0430		
	0434	DMA Xilinx Status Read	
	0438	DMA FIFO data slave read	
	043C	DMA Status read / DMA Status Clear write	
	2XXX	DMA Data Read	
11..7F		spare	

DMA Definitions

DMA Base Control

$0400
Read – Write

Bit#	Definition
0	Reset_0
1	Reset_1
2	Reset_2
3	Reset_3
4	Reset_4
5	spare
6	spare
7	LED Control
8	READ_EN_STD
9	READ_EN_DMA
10	Channel
15-11	spare
16	Int En 0
17	Int En 1
18	Int En 2
19	Int En 3
20	Int En 4
21	Int En 5
22	Int En 6
23	Int En 7
24	Master Interrupt Enable
25	Force Interrupt

Reset_0 when 0 resets the FE Xilinx devices (4). When '1' enables the FE Xilinx devices.

Reset_1 when 0 resets the input FIFOs (16). When '1' enables the Input FIFOs. The FIFOs must be enabled then reset then re-enabled as part of initialization. The clock selection should be to PCI clock for this operation. Please refer to the FE Xilinx description for more details. The Input FIFOs must be reset after the FE devices are enabled to prevent spurious writes to the FIFO when the FE device starts up.

Reset_2 when 0 resets the Latch Xilinx devices (2). When '1' enables the Latch Xilinx devices.

Reset_3 when 0 resets the Address Generator Xilinx devices (2). When '1' enables the Address Generator Xilinx devices.

Reset_4 when 0 resets the Output FIFO devices (4). When '1' enables the Output FIFO devices. The FIFOs must be enabled then reset then re-enabled as part of initialization. The Output FIFOs must be reset after the Latch devices are enabled to prevent spurious writes to the FIFO when the Latch Xilinx starts up.

Int En X. When set ('1') and the corresponding Done bit is received, the interrupt to the host is asserted via the PLX device. The PLX will also have to be enabled to cause an interrupt. The master interrupt within the DMA Xilinx will need to be enabled. Clear the interrupt by clearing the done bit or masking off with the enable. Until the done bit is cleared do not re-enable the interrupt source.

Interrupt master en when 1 enables the DMA Xilinx to assert an interrupt request to the PLX chip and in turn to the PCI bus. The PLX chip has a bi-directional interrupt request line which must be programmed to be an input before setting the Interrupt master en. A logic conflict will exist if the PLX device is not properly programmed. Default is '0'.

Force Int when '1' will cause an interrupt to be set. Also requires Interrupt Master enable and PLX interrupt enable. Useful for software debugging and test purposes. Clear by setting low.

READ_EN_STD when '1' enables the read state-machine in standard mode. The State Machine will poll the empty

flag; when the output FIFO is not Empty data is moved into the holding register. The Valid bit is set when data is ready to be read and cleared when the data is "stale" or not updated.

READ_EN_DMA when '1' enables the read state-machine in the DMA mode. When the PLX device accesses from the DMA read address; the state-machine starts up, and when the Output FIFO of Channel has at least 1/2 FIFO of data will respond to the access by asserting READYn. Data is continuously supplied to the PLX device until BLASTn is asserted. [1 data word per PCI clock to support a burst transfer]. When the burst is completed and BLASTn is asserted the pipeline stops and holds the current data. When additional reads from the DMA read address take place the process restarts with the data in the pipeline. Due to PCI requirements, the burst length is limited to approximately 250 clocks per burst. The FIFO debth is 1K. Starting with 1/2 FIFO guarantees that the FIFO will not run dry during a burst transfer. Channel 0 and 4 are used to Retrieve data. When channel 0 or 4 reaches the "Done" condition so that all requested data is stored into the FIFO the 1/2 full requirement is "waived" to allow the DMA counter in the PLX device to complete the transfer and not get stuck needing less than 1/2 FIFO of data to complete. The length counter in the Address Generator must be coordinated with the PLX DMA count requested. See the Address Generator and Operational section for more information.

Only one of the two reads should be selected at a time. To change modes, select neither then select the channel then select the mode.

Channel when '0' select Output FIFO 0 which corresponds to channels 0-3. When '1' selects Output FIFO 1 corresponding to channels 4-7. Channel should be selected before selecting Read Std or Read DMA. Unexpected results will occur otherwise. Turn off read standard and read DMA. Select channel. Reset FIFO if needed. Enable read mode.

LED Control when '1' will turn on the LED and when '0' will turn off the LED. Rev 02 boards and later.

DMA Status

$043C

Bit#	Definition
0	Done channel 0
1	Done channel 1
2	Done channel 2
3	Done channel 3
4	Done channel 4
5	Done channel 5
6	Done channel 6
7	Done channel 7
8	FIFO_0_Err
9	FIFO_1_Err
10	gnd
11	gnd
12	gnd
13	gnd
14	gnd
15	Interrupt RQST
23-16	SW7-0
24	undefined
25	valid
26	mt_out0n
27	hf_out0n
28	ff_out0n
29	mt_out1n
30	hf_out1n
31	ff_out1n

mt_xn is active low. '0' – FIFO is empty
hf_xn is active low '0' – FIFO is half full or more
ff_xn is active low '0' – FIFO is full.

0 corresponds to channels 0-3, and 1 to channels 4-7.

Done channel X when 1 is done meaning that the requested samples have been transferred. The Data has been captured and stored into SDRAM, or read from SDRAM to the output FIFO as programmed. The done bits are cleared by writing a '1' to the corresponding position. The done bits are used to create an interrupt to the host if the corresponding interrupt enable bit is set. The bits should be cleared after the Xilinx's are enabled from reset to clear any transition induced status changes.

FIFO_X_Err when '1' indicates that the Output FIFO for that channel has become full at some point. In Retrieve mode this is not a problem. In Direct mode this is an overflow error. Clear by writing with the corresponding bit set to '1'.

SW7-0 reflect the settings of the user defined dip-switch on the board. It is envisioned that the switch is used as a board level "address" to identify a specific slot and cable with a particular device number.

DMA FIFO Holding Register Target Read

$0438

Bit#	Definition
31-0	Output FIFO data

Read the data stored within the Output FIFO. Select the Output FIFO to read with the Channel definition. Enable the process with READ_EN_STD. When the valid bit is set, data is stored into the FIFO Holding Register. The data is automatically updated when a read is detected. The hardware overlaps the read of the FIFO and update of the register to reduce the access time from the PCI bus. If the FIFO has data to read, the next data will be available immediately. The valid bit should be used to verify that the first data is available.

DMA FIFO Holding Register DMA Read

$2XXX

Bit#	Definition
31-0	Output FIFO data

Read the data stored within the Output FIFO. Select the Output FIFO to read with the Channel definition. Enable the process with READ_EN_DMA. When enabled and a read to this address occurs the DMA engine within the Xilinx is started. The data is read from the FIFO, stored within the Input FF register and then moved to the Holding register – a three deep pipeline. The initial READY signal is held off until data is ready to be read from the holding register. The data within the register is updated on each clock until the BLASTn signal is asserted by the PLX device. BLASTn will be asserted when the Burst transfer to the PCI bus is halted due to length of transfer or software intervention.

The PLX device requires about 6 clocks to arbitrate for the bus and start the transfer. The max time permitted for a transfer is 256 clocks leaving about 250 data transfers per burst. The transfer is interrupted with the BLASTn signal and the pipeline retains the current contents. The next transfer will begin with the data within the pipeline [shorter start-up sequence within the DMA Xilinx as no prefetch and pipeline fill are required on a restart. In Direct mode, the PLX device will likely have to wait for the DMA process to start-up as the Output FIFO reads happen at a faster rate than the input data from the LVDS front end. During the Process the software should not attempt to access the PCI_LVDS_8R. During Retrieve mode, the Address Generator will stay ahead of the DMA operation; the Output FIFO will always be ready to start a new transfer.

The DMA transfer is controlled by the scatter gather list, PLX device, Address Generator and DMA Xilinx. All must be properly coordinated for effective operation. The Scatter Gather list instructs the PLX where to place data and how much, when to interrupt and when it is completed. The DMA Xilinx selects the group of channels to read from and DMA mode. The Address Generator has a programmed length and address offset to use to define the data to read. The length programmed is in 64 bit words and must be set to provide all of the data requested by the scatter gather list. The scatter gather list will reduce the size of each DMA action and the PCI bus requirements will further subdivide the transfers to be the actual PCI transfers.

DMA Xilinx Status

$0434

Bit#	Definition
0	DN01
1	DN23
2	DN45
3	DN67
4	DNL0
5	DNL1
6	DNA0
7	DNA1

DNx are the done bits from the Xilinx devices. After initialization the Done signal should be '1' if a proper load has taken place.

Address Generator Definitions

Address Generator SDRAM Start Address Registers

0080	ADD0_3	Start ADD CH 0
0084	ADD0_3	Start ADD CH 1
0088	ADD0_3	Start ADD CH 2
008C	ADD0_3	Start ADD CH 3
0180	ADD4_7	Start ADD CH 4
0184	ADD4_7	Start ADD CH 5
0188	ADD4_7	Start ADD CH 6
018C	ADD4_7	Start ADD CH 7

Read – Write

Bit#		Definition
24-0		Initial address to access SDRAM for Channel x
31-25	unused / undefined	

Eight registers at different offsets with the same bit definitions provided for the 0..7 channels.

The Start register is the address to start with for accessing SDRAM. The SDRAM is organized as 64 bit words. The addresses increment with groups of 8 bytes. To select offset 8M bytes the address would be 1M long words. With a range of 24-0 the entire 256 Mb address space is selectable by any channel.

All transfers will start and stop on 64 bit boundaries [by hardware definition]. Smaller transfer requests will be padded to fill a complete word. For example; if an odd number of samples is requested at the front end filter then the data will be padded there to be on a 32 bit boundary. If the number of 32 bit words is odd then the data will be padded onto a 64 bit boundary. There can be up to 3 samples padded in the last line of a capture.

One of the modes re-starts from the end of the last capture [address wise]. The padding occurs with each transfer group so the next starting address will be 64 bit aligned.

In no case are smaller than 64 bit data words written to or read from the SDRAM.

There are no restrictions for page boundaries of the SDRAM. If the initial starting address is placed within x10 before an SDRAM page boundary, then the hardware will process the first part of the transfer as a sequence of individual transfers then go to burst mode at the page boundary. If the length causes the address to cross a page boundary then the pipeline will detect this and stop prior to the page boundary, insert the proper control cycles and restart the burst on the next page. The hardware can handle the different combinations of starting, finishing, and crossing addresses automatically and at full rate as defined in the specification. If attempting to operate outside of the specification, then pay attention to the boundary conditions to increase performance. Pages are 0x00-0x3ff. The memory is sufficiently large that the individual sections can be located on page boundaries. For performance and maintenance reasons page alignment is recommended.

Address Generator SDRAM Length Registers

0090	ADD0_3	Length CH 0
0094	ADD0_3	Length CH 1
0098	ADD0_3	Length CH 2
009C	ADD0_3	Length CH 3
0190	ADD4_7	Length CH 4
0194	ADD4_7	Length CH 5
0198	ADD4_7	Length CH 6
019C	ADD4_7	Length CH 7

Read – Write

Bit#	**Definition**
24-0	Length to access SDRAM for Channel x
31-25	unused / undefined

Eight registers at different offsets with the same bit definitions provided for the 0..7 channels.

The Length register is the number of 64 bit words to transfer into or out of SDRAM. The number of words transferred is N. The count operates from 1<->N providing the transfer length. Because we do not use "0" as a length the address generator can reach 64M-1 [all but 1 64 bit word] words from any one channel in one transfer. With a split transfer the full space can be filled, with multiple channels the full space can be reached. It is intended that the Address Generator defined length control the transfer size. The FE Xilinx should be set to continuous unless in XYZ mode.

Address Generator SDRAM Control Registers

00A0	ADD0_3	CNTL CH 0
00A4	ADD0_3	CNTL CH 1
00A8	ADD0_3	CNTL CH 2
00AC	ADD0_3	CNTL CH 3
01A0	ADD4_7	CNTL CH 4
01A4	ADD4_7	CNTL CH 5
01A8	ADD4_7	CNTL CH 6
01AC	ADD4_7	CNTL CH 7

Read – Write

Bit#	**Definition**
7	Start for Channel x
6-3	unused / undefined mask off for read-back
2	IO – set to 1 for write to SDRAM, 0 for Read
1	DIR – set to 0 for SDRAM capture/retrieve, 1 for Direct
0	Load – set to 0 for preload 1 for start with next address

Eight registers at different offsets; bit definitions provided for the 0..7 channels. The Cntl register starts the transfer for a particular channel, controls whether to pre-load the address, and sets the mode of operation. In multi-channel operation it is important that the active channels are programmed to the same mode. Channel 0 and Channel 4 must be used for retrieve mode. The starting address can be programmed to any location in SDRAM. Only one channel can be read at a time [Retrieve]. Inadvertent retrieve commands to channel[s] 1,2,3

or 5,6,7 will result in an error. The hardware will terminate the operation without doing any transfers and set the done bits for channels 1,2,3 [5,6,7]. Normally only channel 0 or 4 will have the done bit set.

The start bit is read/writeable and resettable. The start bit will, once the SDRAM is initialized and the FIFO is ready, start a transfer or keep one going. The hardware, when the length condition is satisfied, will reset the start bit. 1 = set. If the software resets the start bit prematurely during operation, the current mode is aborted at the next logical opportunity. If a channel is aborted, the done bit is set and the input FIFO is emptied. In capture mode, this data will be written to the SDRAM if the programmed length has not been reached. If the programmed length has still not been achieved, the last word in the FIFO will be repeatedly written to the SDRAM until the desired length has been satisfied. The X_TOTALx_RDBK register can be read to determine the number of valid samples that were written for channel x.

When DIR = 0 the IO bit selects Capture or Retrieve mode of operation. 1 = Capture data from the de-serializer into SDRAM. 0 = Retrieve data from SDRAM to the PCI bus. In capture mode any number of channels can be enabled and any combination of addresses and lengths. In Retrieve mode only channel 0 or Channel 4 should be active. Point the start address at the first channel of interest, set the length and start Retrieve mode. When the data read is completed move the start pointer to the next selection and start channel 0 Retrieve again. The length register does not need to be updated unless a different length is desired.

In capture mode the channels can be started in any order. The state machine revisits the selections periodically and new channels will be added into the processing at that time.

DIR when 1 selects Direct mode. In Direct mode the SDRAM is bypassed with the data flowing from the Input to the Output FIFO. The channel is selected with the start bit active – ONE channel ONLY in this mode. In Direct mode there is no count associated with the transfer. Run until software turns off the start bit and the pipeline empties. Alternatively the FE software done bit can be set to cause the operation to terminate by emptying the Input FIFO.

Load when ‘0’ pre-loads the address stored in the Start register into the address counter for the channel in question when that channel is first accessed for a Capture transfer. If set to ‘1’ then the address is not preloaded and will continue on from whatever was programmed [or not!] previously. It is important to pre-load the initial

access and to pre-load channel 0 after initialization. In Retrieve and Direct mode the pre-load control has no affect.

Address Generator SDRAM Base Control Registers

0x00B0	ADD0_3	SDRAM Base 0-3
0x01B0	ADD4_7	SDRAM Base 4-7

Bit#	Definition
0	Initialize SDRAM 0 = hold inactive, 1 = initialize
1-3	undefined – mask off for read-back
4	swp EEPROM write protect [Memory on SDRAM DIMM]
5	SCL
6	SDA direction 1 = write, 0 = read
7	SDA data

The Control register is used to access the EEPROM supplied on the DIMM if desired and to control initialization. SDRAM supplied in DIMM form comes with an EEPROM installed to allow the operating system to read the DIMM over an I2C bus to determine the characteristics. In this design we ignore the DIMM and can use for general purpose memory. The I2C address is set to '0'. Please refer to I2C and DIMM references for programming the memory.

The SDRAM requires initialization. The initialization involves a pre-charge cycle followed by a register write and then two refresh cycles. The hardware will stay in the low power undefined state until the initialization bit is set high. The SDRAM has an internal register which is controlled by writing to it with the "data" placed on the address lines. Channel 0 has been selected as the initialization source for the "data". **Prior to setting the initialization bit the data 0x27 must be written into the Channel 0 Start register**. During the initialization cycle the 0x27 will be transferred to the SDRAM to set the CAS delay to 2 cycles and the burst size to page size. The hardware automatically will do the pre-charge, register write and refresh cycles. Once the initialization bit is set the software should delay for 2 uS before setting the channel 0 address to correspond to the channel 0 definition. The other channels can be set earlier because they are not involved with initialization. In addition, the SDRAM requires 100 uS of time after the Xilinx removed from reset before the initialization takes place. The Address Generator Xilinx's are held in reset after power-on until the software releases them [DMA Xilinx control]. If software causes a reset at some time after power-on then the reset delay must also be redone before the initialization sequence is performed.

After initialization the hardware enters a series of states called init_refresh where the SDRAM is ready to use but a command has not been detected. A counter delays for 256 clocks then a refresh cycle [4] occurs in an endless loop. When a command [start] has been set then the hardware will begin processing that command. Any combination of channels can be activated. The channels should be activated before the corresponding channels on the Front End Filters in capture mode to make sure that there is not an overflow condition at the Input FIFO.

Address Generator SDRAM Status Registers

0x00BC ADDO_3 Status 0-3

Bit#	Definition
0	Done channel 0
1	mt_0n
2	hf_0n
3	ff_0n
4	Done channel 1
5	mt_1n
6	hf_1n
7	ff_1n
8	Done channel 2
9	mt_2n
10	hf_2n
11	ff_2n
12	Done channel 3
13	mt_3n
14	hf_3n
15	ff_3n
16	gnd
17	mt_outOn
18	hf_outOn
19	ff_outOn

	0x01BC	ADD4_7	Status 4-7
Bit#	**Definition**		
0	Done channel 4		
1	mt_4n		
2	hf_4n		
3	ff_4n		
4	Done channel 5		
5	mt_5n		
6	hf_5n		
7	ff_5n		
8	Done channel 6		
9	mt_6n		
10	hf_6n		
11	ff_6n		
12	Done channel 7		
13	mt_7n		
14	hf_7n		
15	ff_7n		
16	gnd		
17	mt_out1n		
18	hf_out1n		
19	ff_out1n		

The status register reports the Input FIFO status, Done bits from the FE Xilinx, and the Output FIFO status.

mt_xn is active low. '0' – FIFO is empty, hf_xn is active low '0' – FIFO is half full+, ff_xn is active low '0' – FIFO is full.

Done channel X when 1 is done; the requested samples have been captured and loaded into that channel's FIFO. The Done bits are transitory in nature and should not be used to poll [address generator]. The Done bits have a capture and hold circuit within the DMA Xilinx. See DMA Status Register.

FE Definitions

FE Tag Bit Definition Registers

	0000	FE01	TAG_DEF_0
	0030	FE01	TAG_DEF_1
	0040	FE23	TAG_DEF_2
	0070	FE23	TAG_DEF_3
	0100	FE45	TAG_DEF_4
	0130	FE45	TAG_DEF_5
	0140	FE67	TAG_DEF_6
	0170	FE67	TAG_DEF_7

Read – Write

Bit#	**Definition**
1-0	Tag 0 channel Start Save
3-2	Tag1 channel Start Save
5-4	Tag 2 channel Start Save
7-6	Tag 3 channel Start Save
8	Parity Channel Odd / Even
9	Parity Channel On/Off
10	Start Channel
11	Continuous mode
12	Clk Sel
13	Tag Mask
14	Count enable
15	Ch A/B De-serializer enable
31-16	unused / undefined

Two registers at different offsets with the same bit definitions provided for the A and B channels.

Tag Bit definitions : The tag bits are received from the de-serializer as part of the data stream. The received tag bits are decoded using the definitions in the base register. For example if a tag pattern of '00' is received then bits 1,0 are used to determine if the data should be saved or not and if the pattern is a start pattern or not. Each tag pattern, 0,1,2,3 is defined separately for each channel. Any number of tag patterns can be marked for start and storage. $FF would correspond to no filtering with all set for start and save. $00 would correspond to no action as no start bit is selected and no data set for storage. A more normal situation would be to select a subset of patterns for start and storage. Please note that the start pattern is not saved unless it is marked to be saved.

Parity : The parity is programmable to be odd or even and to be inserted or not. The odd data bits [1,3,5,7,9,11,13] are used to determine the parity generation for bit 15. The even parity bits are used to determine the parity generation for bit 14. If parity is not enabled then '0' is inserted in the parity bit locations.

Start : once the stop values are set the base register can be written to with the tag, parity, clock selection, de-serializer enable and start action. The Start bit is set by software to initiate operation and cleared at the end of the sequence programmed. The start bit can be polled to see if the data capture has completed at the Filter. The start bit can be cleared with software to halt the continuous mode.

Continuous : The mode is determined by the stop values programmed and the Continuous bit. If the Continuous bit is set then the stop values are ignored and all programmed values are captured. If all values are desired then $FF should be programmed into the mode bit definitions. The mode is halted by resetting the start bit. It is recommended to use the continuous mode for all non-XYZ mode captures and to use the length counter in the Address generator to control the amount of data captured. In X-Y-Z mode the length of the programmed data captured by the FE chip should be greater or equal to the amount programmed into the Address generator length for that channel. If a smaller amount of data is provided by the FE chip then the Address Generator will pad the data out to the length requested. The done bit will be set by the FE chip when the XYZ sequence is completed and the Address Generator will interpret that to mean that the last of the data is in the FIFO and read it all out. If the FIFO becomes empty the Address Generator will re-read the last sample from the FIFO until it completes the capture operation. Usually this is not what is intended.

Clock Select : When 0 the PCI clock is used instead of the de-serializer clock. When 1 the de-serializer clock is used. Select the PCI clock to use the load FIFO mode. To fill a specific value into all of SDRAM, write the value to the holding register, select the PCI clock, and start a capture with X set to max size and the memory controller set to have the channel selected start at 0 and occupy the entire space. The data is muxed into the pipeline at the last stage when the select bit is '0' and the Count enable bit is '0'.

Count Enable: When '1' enables the 12 bit counter to count. When the PCI clock is selected then the counter output is muxed into the data stream prior to word building. If the tag bits are set to 0xff, the continuous mode selected, start bit set [0x4cff] then the counter data will be inserted into the data stream and the state-machine will not add the parity leaving the counter output as the data stream. The count is pre-loadable. The pipeline will absorb the first few counts. Starting with 0x000 preloaded will yield 0x00040003 loaded into the Input FIFO.

De-serializer enable : When '0' the de-serializer is in power down mode. When '1' the de-serializer is enabled. The de-serializer should be enabled prior to selecting the de-serializer clock. The PLL in the deserializer takes 10 mS to stabilize assuming there is an active clock reference on the serial input. There must be a delay after enabling the channel before starting a capture. The de-serializer cable can be detected as active by reading the X Total counter back while the data is being captured. If the counter is not progressing then there is no reference clock. Select all patterns for start and save to keep the counter responding to each clock that is received.

Tag Mask : When '0' the tag bits are forced to '0' for storage purposes only. The tag bits are still used to determine which samples to start and save. '1' corresponds to saving the tag bits.

FE X Stop Registers

0004	FE01	X0_STOP
0008	FE01	X1_STOP
0044	FE23	X2_STOP
0048	FE23	X3_STOP
0104	FE45	X4_STOP
0108	FE45	X5_STOP
0144	FE67	X6_STOP
0148	FE67	X7_STOP

Xx Stop : Read – write
26 – 0 set the number of samples to capture per X loop.

FE Y Stop Registers

000C	FE01	Y0_STOP
0010	FE01	Y1_STOP
004C	FE23	Y2_STOP
0050	FE23	Y3_STOP
010C	FE45	Y4_STOP
0110	FE45	Y5_STOP
014C	FE67	Y6_STOP
0150	FE67	Y7_STOP

Yx Stop : Read – write
20 – 0 set the number of samples to skip after capturing X before looping. If not in a loop mode then should be set to 0.

FE Z Stop Registers

0014	FE01	Z0_STOP
0018	FE01	Z1_STOP
0054	FE23	Z2_STOP
0058	FE23	Z3_STOP
0114	FE45	Z4_STOP
0118	FE45	Z5_STOP
0154	FE67	Z6_STOP
0158	FE67	Z7_STOP

Zx Stop : Read – Write
20 – 0 set the number of loops of X and Y to implement. If Y is not set then use a larger X value and program to 0.

Please note that all three stop values count from 0 to the value programmed – $F is 0 through F for a total of 16…program in "N-1" to get the count that you desire.

FE X Total Counter Read-back

001C	FE01	X_TOTAL_0_RDBK
0020	FE01	X_TOTAL_1_RDBK
005C	FE23	X_TOTAL_2_RDBK
0060	FE23	X_TOTAL_3_RDBK
011C	FE45	X_TOTAL_4_RDBK
0120	FE45	X_TOTAL_5_RDBK
015C	FE67	X_TOTAL_6_RDBK
0160	FE67	X_TOTAL_7_RDBK

X Total x Counter : Read only
Read the total number of stored samples count value. The count value is double clocked and held to be stable with the PCI based clock. Counter occupies data bits 26 – 0. Please note that the counter resets to 0 at the beginning

of a new acquisition and keeps a cumulative count of the number of samples written to the input FIFO. When running in direct mode with a continuous stream of input data the counter will roll over after 0x7ffffff samples have been written to the input FIFO. In capture mode this is the size of one SDRAM bank, so it is the maximum amount that can be written to any one channel.

FE Data Holding Register

0024	FE01	0,1_DTA_PAT
0064	FE23	2,3_DTA_PAT
0124	FE45	4,5_DTA_PAT
0164	FE67	6,7_DTA_PAT

FIFO Write Register : 31 – 0 write only. Value to write to FIFO. Can be written once to the register then loaded multiple times or re-written to a new value for each FIFO write. The data is muxed into the data pipeline when the PCI clock is selected. The PCI clock needs to be selected to have proper operation when writing directly to the FIFO.

FE Data Write Register

0028	FE01	FIFO_0 WRT
002C	FE01	FIFO_1 WRT
0068	FE23	FIFO_2 WRT
006C	FE23	FIFO_3 WRT
0128	FE45	FIFO_4 WRT
012C	FE45	FIFO_5 WRT
0168	FE67	FIFO_6 WRT
016C	FE67	FIFO_7 WRT

FIFO x Write : no data required **read** only. When accessed the data in the FIFO Write Register is moved to the FIFO for the corresponding channel. Useful for self test and pre-loading the SDRAM. For pattern and multiple location fills it is recommended to use the counter and capture modes instead – much faster.

FE Channel Done

0034	FE01	FE_DONE_0
0038	FE01	FE_DONE_1
0074	FE23	FE_DONE_2
0078	FE23	FE_DONE_3
0134	FE45	FE_DONE_4
0138	FE45	FE_DONE_5
0174	FE67	FE_DONE_6
0178	FE67	FE_DONE_7

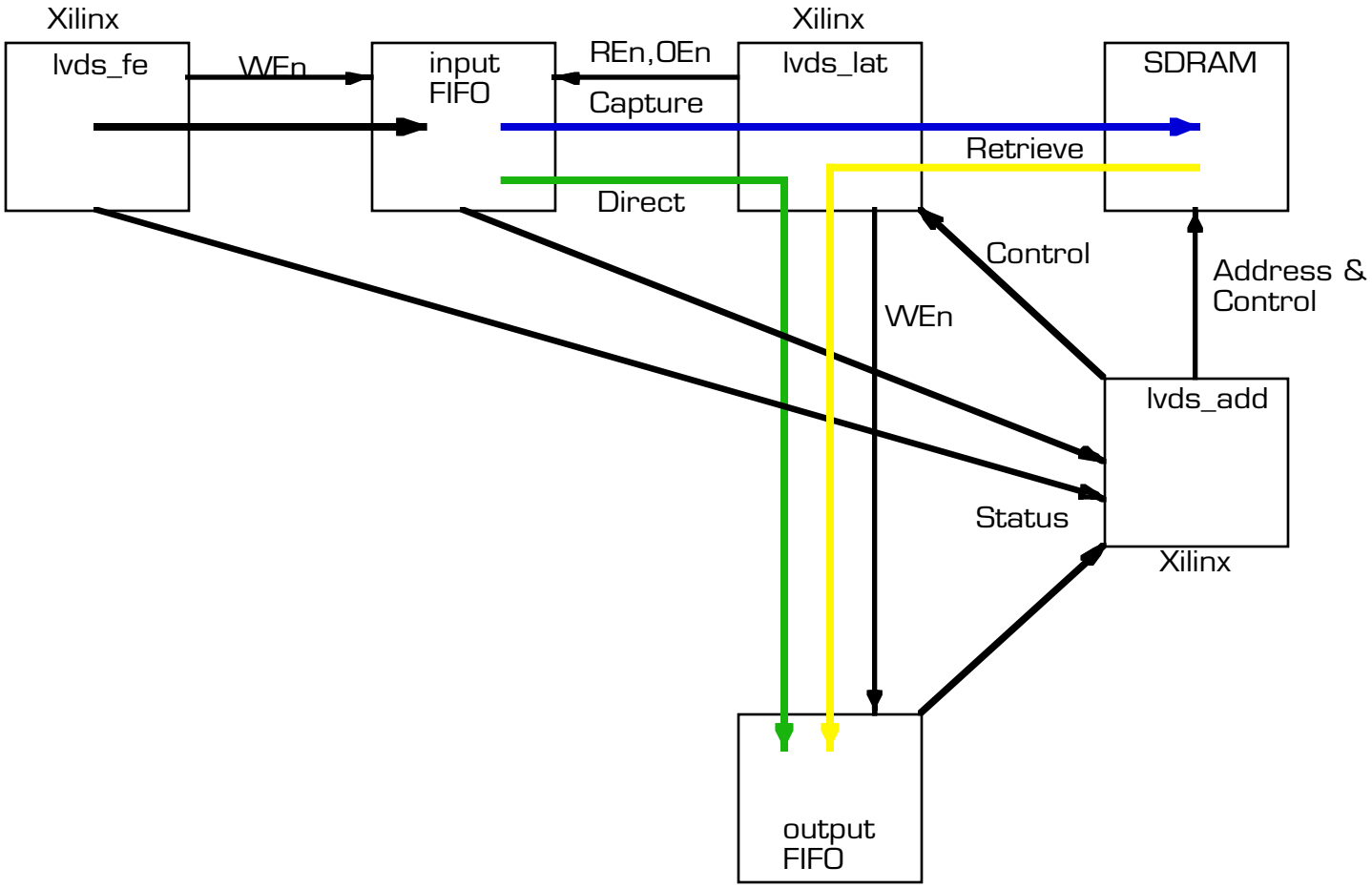
Writing to the "Done" register for a channel will force a Done signal to be sent to the Address generator for that channel. The Done bit will signal the completion of an operation. Useful to force completion. Example : load data with software data definition and load commands into the FIFO, Start-up the Address generator to move in direct mode to the Output FIFO. Set the Done bit to cause the Address generator to read the last portion of data from the Input FIFO. Use the bit to abort without loosing data. Stop the process then use the done bit to complete and keep what is in the FIFO.

FE Pre-load Counter

	003C	FE01	Preload data counter 0-1
	007C	FE23	Preload data counter 2-3
	013C	FE45	Preload data counter 4-5
	017C	FE67	Preload data counter 6-7
27-16	load 1,3,5,7		
11-0	load 0,2,4,6		

A write to the Pre-Load Counter address will load the counters with the start pattern. The lower [Channel A] counter will be loaded with the 11-0 data bits and the upper [channel B] will be loaded from 27-16. The counters when enabled will start to count from this pattern. The load function has higher priority than the count function. A write while already enabled will reset the counter to the written value [for one clock, then counting will begin again]. Load a '0' to clear the counter. Counter used for loading patterns into the FIFO for various test capabilities.

Operational Brief:



In Capture mode the Address Generator hardware waits for the combination of an active channel request [start] and the half full status true condition from the corresponding input channel. When data is present the state machine will begin to transfer the data from the input FIFO to the SDRAM. The transfers occur with burst accesses as much as possible. The state machine loops, checking each channel for activity, then refreshing and looping again until all channels are completed. The Input FIFO is filled based on the LVDS data and the tag bit definitions.

The Address Generator should be programmed for the active channel(s). The starting address and length first then the start commands. Once the Address generators are started the FE devices can be programmed and started. The FE registers should be programmed for length, clock selection, deserializer enable, tag bits, parity and so forth first. The start bit can be set once the other registers and any required delay for the deserializer taken care of. If the DMA Xilinx is programmed to generate an interrupt based on the done bits then the host will be interrupted when the various channels complete. Alternatively the done bits can be polled.

In Retrieve mode the data is read from the SDRAM and written to the output FIFO. Data is transferred 256 long words to a burst. The state machine will keep from just under 1/2 full to full in the output FIFO by monitoring the HF flag and bursting when there is room. The DMA controller will attempt to empty the FIFO to the PCI bus at the same time. The Address generator has the advantage of 2X bandwidth and will be able to keep the DMA process from running out of data. Channel 0 is used to Retrieve data from the SDRAM for channels 0-3 and channel 4 is used to control Retrieve for channels 4-7.

First the DMA Xilinx is programmed to select the correct channel and mode. The Output FIFO should be reset if not empty. The Address Generator should be programmed for channel 0 or 4. The starting address and length first then the start commands. Once the Address generators are started the data will be transferred to the Output FIFO on a space available basis. If DMA is used the PLX will start the transfer by getting the scatter gather from host memory then reading from the DMA address in the DMA Xilinx. The transfer will continue until the scatter gather list is exhausted. Any number of longwords can be moved from the SDRAM to the PCI bus. The count in the PLX device will control the total length. If more data is in the scatter gather list than is requested from the Address Generator the last data will be repeated until the list is completed…be careful to program the length properly to match the 64 bit count with the byte count that the PLX uses.

In Direct mode data is moved from the Input FIFO to the Output FIFO bypassing the SDRAM. The half-full flag is used to determine when there is data in the Input FIFO. The clock rate and number of accepted samples will determine the captured data rate. The Output FIFO may go empty between bursts on the PCI bus. The PLX device will be held off until sufficient data is stored within the Output FIFO to start a new PCI burst. The PLX device will not capture the PCI bus until the internal FIFO has data. [the hardware will not lock up the bus waiting for data] The PCI bus has a 2x advantage over input data stream. If the data is not read in time from the Output FIFO to be able to accept new data from the Input FIFO then data will be lost. The Output FIFO should never become Full. Status bits are set [DMA status register] to provide error feedback from this potential condition.

The Hardware should be initialized DMA first, Output FIFO reset second, Address generator third, FE fourth, PLX last. The PLX chip can be initialized all but the last step of enabling the DMA function before doing the Xilinx definitions. Once the FE Xilinx's are started the data can begin to flow through the board. The PLX device must be ready to handle the data when it arrives to prevent an overflow condition. Direct mode mode only. In Direct mode there will be [513 + 1023] x 2 x 40 nS = 122.88 uS to capture enough samples to cause overflow once the FE is enabled. [1/2 + 1 at input FIFO, all but one in output FIFO, 2 samples per word, 25 mhz capture rate]. There is plenty of time for the PLX to fetch the 4 parameters from main memory and to start-up in time to transfer the data.

The PLX device should be programmed to start the DMA transfer with the first sample read from the DMA Xilinx and to read new data whenever there is at least room for 8 data samples in the internal FIFO. The PLX will then start-up when commanded, wait for the DMA Xilinx to respond [FIFO is half full on programmed channel and state-machine has started up] then request the PCI bus when the first transfer has happened from the DMA Xilinx. The Bus arbitration and start-up take 6 clocks, during which time 6 more samples will have been read from the DMA Xilinx. Assuming that the PCI bus is not busy, delaying the start of the burst, the DMA Xilinx and the PCI bus will be synchronized and data will flow from the Output FIFO through the DMA Xilinx and PLX device to the PCI bus. If the PCI bus has an issue or the max time has expired the PLX device will issue a BLASTn signal to the DMA Xilinx to halt the transfer. When there is room within the PLX FIFO the process will restart. The pipeline will retain the previous state and begin again where it left off. If the PCI bus is not used by other devices; the only down time will be the 6 clocks for arbitration plus an additional 3 within the DMA Xilinx to restart. 250 data samples per 250+9 clocks for an effective bandwidth of 127.4 Mbytes/Sec. The SDRAM can support the data rate in Retrieve mode.

LVDS Connector Definition

[3M N102A0-52E2VC]

Pin	Signal Name	Alternate Name
1	GND*	
2 – 9	SPARE	
10	CH6RXCLKP	06_CLK_T
11	CH6RXCLKM	06_CLK_C
12	CH6RX2P	
13	CH6RX2M	
14	CH6RX1P	06_UDATA_T
15	CH6RX1M	06_UDATA_C
16	CH6RX0P	06_LDATA_T
17	CH6RX0M	06_LDATA_C
18	GND*	
19	GND*	
20	CH4RXCLKP	04_CLK_T
21	CH4RXCLKM	04_CLK_C
22	CH4RX2P	
23	CH4RX2M	
24	CH4RX1P	04_UDATA_T
25	CH4RX1M	04_UDATA_C
26	CH4RX0P	04_LDATA_T
27	CH4RX0M	04_LDATA_C
28	GND*	
29	GND*	
30	CH1RXCLKP	01_CLK_T
31	CH1RXCLKM	01_CLK_C
32	GND*	

33	CH1RX2P	
34	CH1RX2M	
35	CH1RX1P	O1_UDATA_T
36	CH1RX1M	O1_UDATA_C
37	CH1RXOP	O1_LDATA_T
38	CH1RXOM	O1_LDATA_C
39	GND*	
40	GND*	
41	CHORXCLKP	OO_CLK_T
42	CHORXCLKM	OO_CLK_C
43	CHORX2P	
44	CHORX2M	
45	CHORX1P	OO_UDATA_T
46	CHORX1M	OO_UDATA_C
47	CHORXOP	OO_LDATA_T
48	CHORXOM	OO_LDATA_C
49	GND*	
50	GND*	
51-60	SPARE	
61	CH7RXOM	O7_LDATA_C
62	CH7RXOP	O7_LDATA_T
63	CH7RX1M	O7_UDATA_C
64	CH7RX1P	O7_UDATA_T
65	GND*	
66	CH7RX2M	
67	CH7RX2P	
68	CH7RXCLKM	O7_CLK_C
69	CH7RXCLKP	O7_CLK_T
70	GND*	
71	GND*	
72	CH5RXOM	O5_LDATA_C

73	CH5RXOP	O5_LDATA_T
74	CH5RX1M	O5_UDATA_C
75	CH5RX1P	O5_UDATA_T
76	CH5RX2M	
77	CH5RX2P	
78	CH5RXCLKM	O5_CLK_C
79	CH5RXCLKP	O5_CLK_T
80	GND*	
81	GND*	
82	CH3RXOM	O3_LDATA_C
83	CH3RXOP	O3_LDATA_T
84	CH3RX1M	O3_UDATA_C
85	CH3RX1P	O3_UDATA_T
86	CH3RX2M	
87	CH3RX2P	
88	CH3RXCLKM	O3_CLK_C
89	CH3RXCLKP	O3_CLK_T
90	GND*	
91	GND*	
92	CH2RXOM	O2_LDATA_C
93	CH2RXOP	O2_LDATA_T
94	CH2RX1M	O2_UDATA_C
95	CH2RX1P	O2_UDATA_T
96	CH2RX2M	
97	CH2RX2P	
98	CH2RXCLKM	O2_CLK_C
99	CH2RXCLKP	O2_CLK_T
100	GND*	

GND* = AC, DC, Open connection to Ground. Standard = open.

Construction and Reliability

PCI Modules were conceived and engineered for rugged industrial environments. The PCI_LVDS_8R is constructed out of 0.062 inch thick FR4 material. The connector bezel and extender bracket provide support at both ends of the card in addition to the PCI connector.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components.

Thermal Considerations

The PCI_LVDS_8R design consists of CMOS circuits. The power dissipation due to internal circuitry other than the SDRAM is very low. Forced air cooling is recommended. Commercial temperature components are utilized. 0-70 C is the case temperature range for these components. Sufficient forced air is required to provide adequate cooling to keep the component temperatures within normal operating limits. In most chassis very minimal air flow will be required. The airflow required will be a function of the temperature of the cooling air, and the amount of heat to dissipate from the PCI_LVDS_8R and the other cards installed into the same chassis.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

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purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering

435 Park Dr.
Ben Lomond, CA 95005
831-336-8891 831-336-3840 fax
e-mail support@dyneng.com

Specifications

Logic Interface:	PCI 2.1, 32 bit 33 MHz. PLX 9054
LVDS Interface:	8 Channels of receive: Clock, Serial 0, Serial 1 implemented based on National DS90CR218. TIA/EIA-644 compliant. 175 MHz. Serial data rate per serial channel – 14 bits at 25 MHz. Internal. Options for 21 bit interface.
Software Interface:	Control Registers, Status Registers
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	DMA and target
Interrupt:	Programmable interrupt based on each separate channel.
Onboard Options:	All Options are Software Programmable
Interface Options:	3M LVDS Connector MDR Series 100 pin
Dimensions:	Standard Full Length PCI Card
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Power:	Either 3.3 or 5V power source. Theoretical Max. 7A. Typical max = 4.4A. Voltage selectable with inductor placement. See order information.

Order Information

The PCI_LVDS_8R board has 2 standard configurations.
http://www.dyneng.com/pci_lvds.html

"**no dash"**	PCI full length card with connector bezel and extender bracket 8 LVDS Channels with 512MB SDRAM DMA and Target operation Universal voltage 32 bit / 33 MHz PCI interface 3.3V power supply utilized
"-1"	Same as no dash version plus on board regulator used to convert 5V to 3.3.
Tools for PCI_LVDS_8R	Engineering Kit - PDF of schematic, Reference Software including "C" source that we use for testing the design [NT, WinRT environment], LVDS Cable, MDRterm100 [LVDS breakout connector with testpoints]
	Driver – Windows NT compatible driver for PCI_LVDS_8T