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PCI-LVDS-2T

2 Channel Lvds
Serial Transmit Interface

Revision A1
Corresponding Hardware
PCI-LVDS-2T: Revision C/D 10-2001-0903/0904

PCI-LVDS-2T
2 Channel Lvds Serial Transmitter

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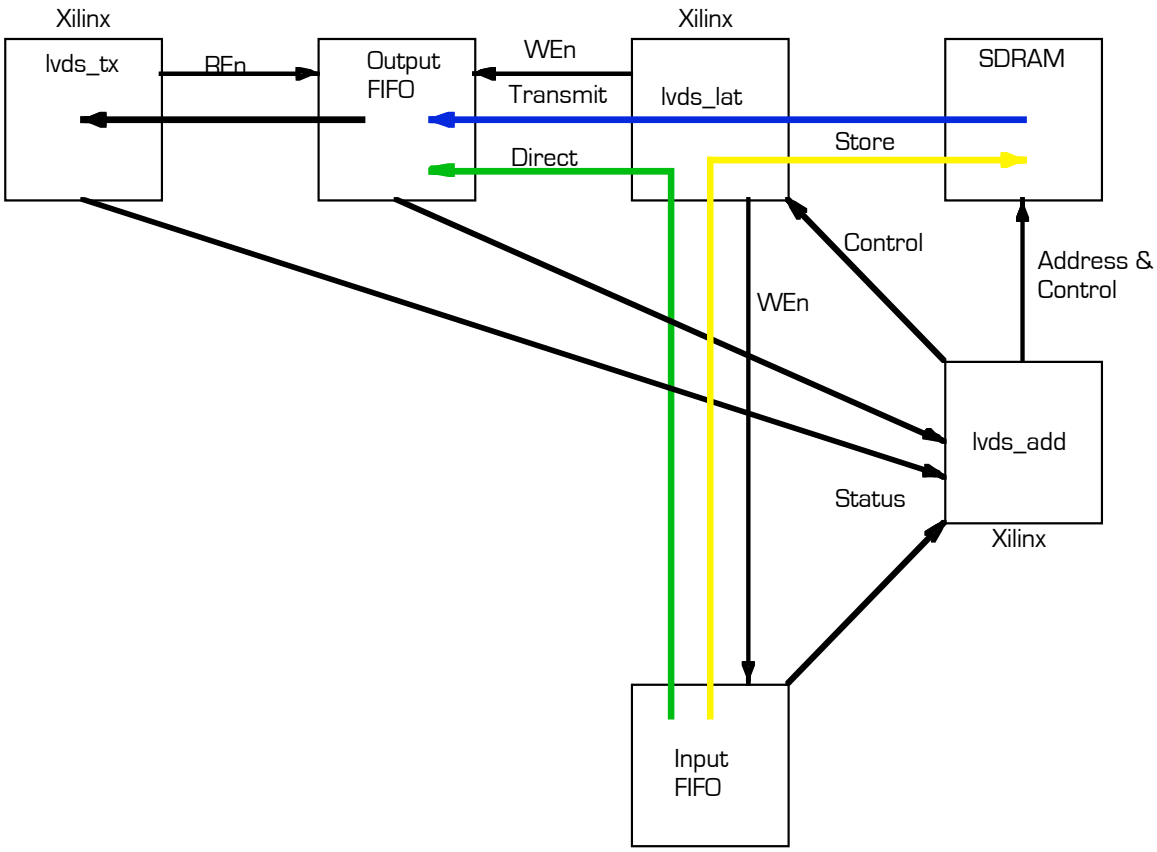

FIGURE 1 PCI_LVDS_2T DATA FLOW DIAGRAM

The PCI_LVDS_2T has three basic modes of operation: data can be stored (store) into the bulk memory (SDRAM]; data can be retrieved from the SDRAM and transmitted (transmit]; or data can be directly sent from the PCI interface to the output (direct]. These data-flow modes are supported by FIFOs and embedded state-machines.

There are 2 channels of LVDS supported. Each LVDS channel is controlled by one of the two “TX” Xilinx’s. The TX Xilinx will read the data from the Output FIFO, convert from 32-bit to 21-bit data, do the final data processing and stay in synchronization with the LVDS reference clock. Each of the LVDS channels has a separate Output FIFO.

The Output FIFO is sourced from the Input FIFO or the SDRAM via the Latch Xilinx. One Latch Xilinx supports each LVDS channel. There are two Latch

Xilinx installed per PCI_LVDS_2T. The Latch Xilinx provides the data bus width increase and reduction to match the 32-bit FIFOs with the 64-Bit SDRAM. The Data path between the FIFOs operates at 66 MHz and the path between the Latch and the SDRAM operates at 33 MHz. The Latch design is controlled by the Address Generator Xilinx.

The Address Generator Xilinx creates the control for the SDRAM and Latch Xilinx devices. The Address Generator creates the start-up sequence, refresh, burst read and burst write controls for the SDRAM, plus the control signals for the Latch Xilinx.

The Address Generator works with a round-robin arbitration scheme looking at the Output FIFO's half-full flag and start bit to determine which channel to transfer to next. Data is moved into the Output FIFO at 66 MHz as 32-bit data. Data is removed as 32-bit data at 25 Mhz (Max] giving the Address Generator more than 2:1 ratio on any one channel providing the necessary margin to support the 1 channel per Address Generator plus the SDRAM overhead (refresh and arbitration]. There are two Address Generator Xilinx's per PCI_LVDS_2T.

There are a total of seven Xilinx devices on the board, including the DMA Xilinx, which handles the basic decoding for the board and the DMA interface into the Input FIFO.

The modes of operation are supported by clocking and starting options. Internal and external clock and start pulses can be used to control the frequency and synchronization.

The ‘2T can select the FP (front panel], RP (rear panel] or on-board clock references. A typical configuration would be to use the FP input to one card within a chassis and route that to the RP. The rest of the cards within the chassis can use the RP connectors for clock distribution. The FP connectors can be used between chassis and the RP within the chassis for clean wiring. The clock and start-pulse distribution is accomplished with LVDS drivers and receivers plus high-speed multiplexers for a low-skew distribution architecture.

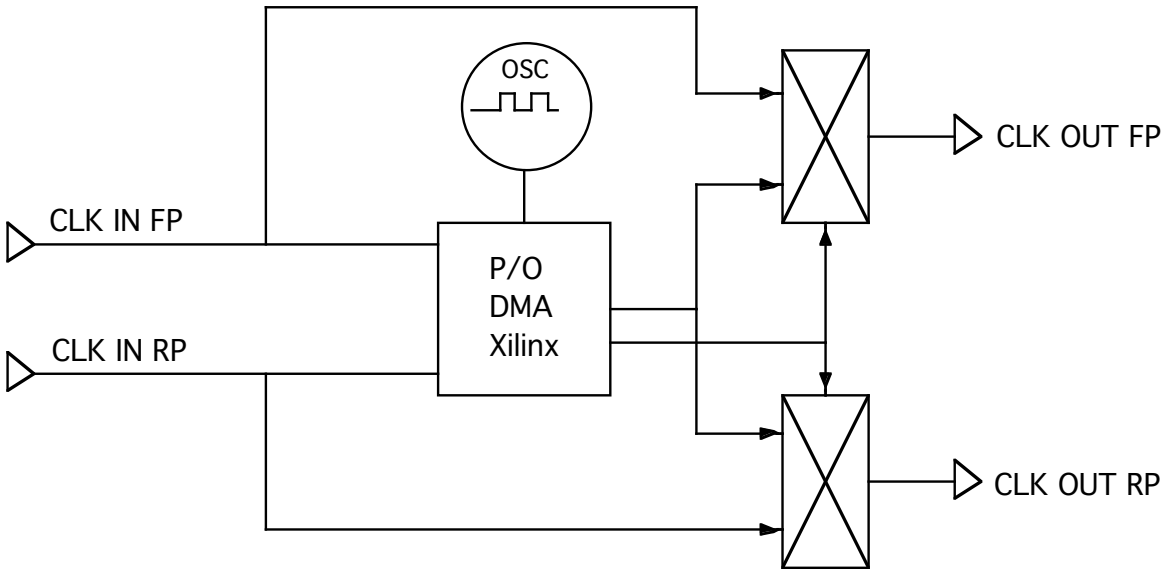

FIGURE 2 PCI_LVDS_2T CLOCK DISTRIBUTION

The external trigger has a similar mechanism for distribution. The external trigger pulse is synchronized to the reference clock and distributed directly to the TX Xilinx devices. The local trigger can be generated via a software command or external triggers can be used to allow for master-slave chaining. The FP external trigger is routed to the DMA Xilinx to allow an external trigger to be routed through to the RP connector.

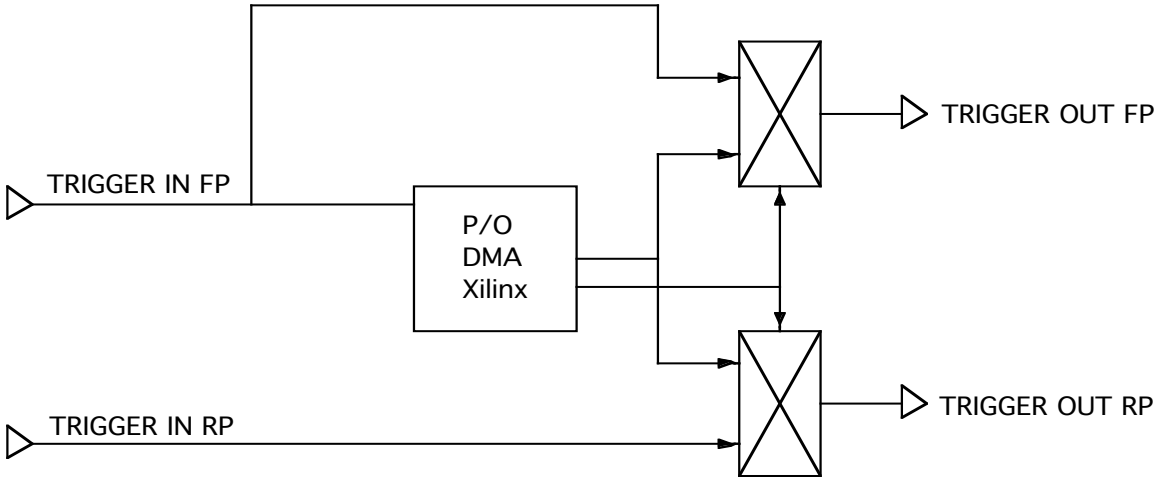

FIGURE 3 PCI_LVDS_2T TRIGGER DISTRIBUTION

Memory Map

TX Channel 0

Decode number	Address offset	Chip	Definition
0	0000	TX01	CNTL_STAT_0
	0004	TX01	DATA_RDBACK_0
	0008	TX01	W_COUNT_0
	000C	TX01	X_COUNT_0
	0010	TX01	Y_COUNT_0
	0014	TX01	Z_COUNT_0
	0018	TX01	IDLE_0_0
	001C	TX01	IDLE_1_0

Address Generator Channel 0

Decode number	Address offset	Chip	Definition
2	0080	ADD0_3	ADD CH 0 A
	0090	ADD0_3	ADD CH 0 B
	00A0	ADD0_3	ADD CH 0 C
	00B0	ADD0_3	ADD CH 0 D

TX Channel 4

Decode number	Address offset	Chip	Definition
4	0100	TX45	CNTL_STAT_4
	0104	TX45	DATA_RDBACK_4
	0108	TX45	W_COUNT_4
	010C	TX45	X_COUNT_4
	0110	TX45	Y_COUNT_4
	0114	TX45	Z_COUNT_4
	0118	TX45	IDLE_0_4
	011C	TX45	IDLE_1_4

Address Generator Channel 4

Decode number	Address offset	Chip	Definition
6	0180	ADD4_7	ADD CH 4 A
	0190	ADD4_7	ADD CH 4 B
	01A0	ADD4_7	ADD CH 4 C
	01B0	ADD4_7	ADD CH 4 D

PLX Interface, Decode and Control

Decode number	Address offset	Chip	Definition
10	0400	DMA	Base Control r-w
	0404	DMA	Timing Control r-w
	0434	DMA	Xilinx done status
	0438	DMA	FIFO slave write
	043C	DMA	Status read
	043C	DMA	Status clear write
	2XXX	DMA	Data DMA write

DMA Definitions

DMA Base Control

0x400
Read – Write

Bit#	Definition
0	RESET_0
1	RESET_1
2	RESET_2
3	RESET_3
4	RESET_4
6-5	spare
7	LED control
8	WRITE_EN_STD
9	WRITE_EN_DMA
10	CHANNEL
15-11	spare
16	INT_EN_0
20	INT_EN_4
24	INTERRUPT_MASTER_ENABLE
25	FORCE_INT

RESET_0 when ‘0’ resets the TX Xilinx devices (2); when ‘1’ enables the TX Xilinx devices.

RESET_1 when ‘0’ resets the Output FIFOs (4); when ‘1’ enables the Output FIFOs. The FIFOs must be enabled then reset then re-enabled as part of initialization. The clock selection should be the PCI clock for this operation. Please refer to the Clock Control description for more details.

RESET_2 when ‘0’ resets the Latch Xilinx devices (2); when ‘1’ enables the Latch Xilinx devices.

RESET_3 when ‘0’ resets the Address Generator Xilinx devices (2); when ‘1’ enables the Address Generator Xilinx devices.

RESET_4 when ‘0’ resets the Input FIFO devices (4); when ‘1’ enables the Intput FIFO devices. The FIFOs must be enabled then reset then re-enabled as part of initialization.

INT_EN_X when set (‘1’) and the corresponding done bit is active the interrupt to

the host is asserted via the PLX device. The PLX will also have to be enabled to cause an interrupt and the master interrupt within the DMA Xilinx will need to be enabled. Clear the interrupt by clearing the done bit or masking off the enable. Until the done bit is cleared do not re-enable the interrupt source.

INTERRUPT_MASTER_ENABLE when '1' enables the DMA Xilinx to assert an interrupt request to the PLX chip and in turn to the PCI bus. The PLX chip has a bi-directional interrupt request line which must be programmed to be an input before setting the master interrupt enable. A logic conflict will exist if the PLX device is not properly programmed. Default is '0'.

FORCE_INT when '1' will cause an interrupt to be set. Also requires Interrupt Master enable and PLX interrupt enable. This bit is useful for software debugging and test purposes. Clear the condition by setting this bit low.

WRITE_EN_STD when '1' enables the write state-machine in standard mode. The State Machine will move data from the internal register to the FIFO when a slave write is detected. The Channel and enable must be set appropriately prior to the writing.

WRITE_EN_DMA when '1' enables the write state-machine in the DMA mode. When the PLX device accesses the DMA write address space, the state-machine starts up and asserts READYn. Data is continuously supplied by the PLX device until BLASTn is asserted (1 data word per PCI clock to support a burst transfer]. When the burst is completed and BLASTn is asserted the PLX has completed the burst write. There are still two data words within the internal pipeline. The state-machine will transfer the last two words then return to wait for the next burst. The state-machine assumes that the address generator has been started prior to the DMA – there will always be room within the Input FIFO. The FIFO error (see status register] indicates that the FIFO went full at some point. When additional writes to the DMA write address take place the process restarts. Due to PCI requirements the burst length is limited to approximately 250 clocks per burst. The fill rate is the PCi rate = 33 Mhz and the transfer rate to SDRAM is 66 MHz.

Only one of the two write modes should be selected at a time.
CHANNEL when '0' selects Input FIFO 0 which corresponds to channel 0; when '1' selects Input FIFO 1 corresponding to channel 4. Channel should be selected before selecting Write Std or Write DMA. Unexpected results will occur otherwise.

LED Control when '1' will turn on the LED and when '0' will turn off the LED.

DMA Timing Control

0x404
Read – Write

Bit#	Definition
0	pulse out enable (pls_out_en]
1	master enable ‘1’ = enabled, ‘0’ = disabled
2	master_slave (mas_slv]
3	spare
4	pulse out select ‘1’ - FP trigger/’0’ - local pulse
15-5	spare
27-16	clock divisor
28	RS – clock post selector
29	spare
31-30	PS – clock source pre-selector

Clock Pre-Selector mapping

00	oscillator
01	front panel (FP) external clock source
10	rear panel (RP) external clock source
11	PCI clock

The clock pre-selector is used to select which clock source to use for the clock reference.

Divisor (11-0) are the clock divisor select bits. The clock source is divided by a counter. The output frequency is {reference / (2*(n+1))}. N≥1. The reference oscillator is 16.56 MHz. The counter divides by N+1 due to counting from 0 ->n before rolling over. The output is then divided by 2 to produce a square wave output.

Post Selector when '1' sets clock out to clock divided, when '0' sets clock out to pre-selector reference clock. When operating with the oscillator or external sources the undivided option is usually correct. When selecting the PCI source the divider should be used.

MAS_SLV when ‘0’ sets the hardware to slave mode. In slave mode the Start pulse is received, buffered, and retransmitted out along with the reference clock at each of the external connectors. The clocks are also routed to the DMA Xilinx to be used as references locally. In Master mode the clock and start-pulse inputs are ignored and the local version is driven off board. Please note that the TX parts will need to be properly programmed for clock source and enable. The default value is slave. It is intended that all boards except the one designated

master are slaves. The source of the clock is selected separately. To receive a clock from the FP and distribute to the RP connector; choose the master designation and set the clock pre-selector to use the FP reference clock.

Master_En when '1' provides a local master enable to the TX FPGAs. The Master enable for each board should be set after the Add_Gen and TX devices are programmed. If the TX parts are programmed to wait for an external trigger, then the master_en will enable the channels to react to the external trigger. When the external trigger is received, multiple cards can be synchronized to transmit together. If the channels are programmed to operate without an external trigger then the local channels will be enabled together with a common clock allowing for coherent start-up across 2 channels.

The source for the driven external triggers is selectable. When in master mode the external trigger is driven from a local source. The **Pulse Out Select** bit is used to select the external FP trigger (in) or the local Pulse Out En source. The purpose for the selection is to allow the FP trigger to be used as the source and the RP and FP outputs driven from that source. An external master trigger can then be used to control a chassis without having to wire to all of the FP connectors. The RP headers can be used for a low skew, "neat" wiring implementation. If the Pulse Out Select bit is cleared then the local Pulse Out En generated pulse can be used to cause a synchronous start-up across multiple cards.

When **Pulse Out Select** = '1' the Master_En is held off until the FP external trigger is received. When the trigger is received the Master_En is asserted along with the PLS_OUT. The added Flip-Flop in the path on the slave cards is accounted for with a 1 clock skew between the Master_En and PLS_OUT. When the channels have completed the transmission, the Master_En should be set to '0', then '1' to rearm for the next external trigger pulse.

When **Pulse Out Select** = '0' the internal controls govern. Master_en is driven when it is set (no hold-off) and Pulse_Out_En controls the Pulse Out signal.

PLS_OUT_EN when set causes a pulse to be generated. If in Master mode this pulse is driven off card to provide a start pulse for external hardware. The master enable for the local channels should be set at the same time on the card designated as master. The local TX parts will use the master enable. The slave cards will use the start pulse. The pulse enable is self-clearing. Set to '1' to cause the pulse.

To use an external clock and trigger from the front panel and with rear panel distribution make the following selections:

1. Select one card for the point of entry and designate that as the master.
2. Set the remaining cards to slaves.
3. Select the FP clock reference on the master card.
4. Select the RP clock reference on the slave cards (or FP if desired to use that connector).
5. Set Pulse Out Select = '1' on the Master card and = '0' on Slave cards.
6. Set the TX chips to wait for the external trigger on slave cards (select RP or FP depending on your wiring).
7. Set the TX chips on the master card to start with the local master enable.

The PCI_LVDS_2T is designed to offset the master enable from the trigger out signal to account for the input FF (synchronization stage) that the slave cards have. All cards can start on the same clock. The clock itself will have skew due to the transmission chain. The specification for the design - 4 clock periods across cards is met under all conditions.

The LVDS receivers and Drivers are fast, and do have an inherent delay. Using the FP or RP distribution will create a delay between the cards. The individual cards re-synchronize the trigger pulse in parallel with the buffering. The LVDS driver has 1.5 nS max delay, the LVDS receiver has 2.5 nS max delay, and the MUX adds 0.25 nS plus trace length of less than 1 nS => plus cable delay ~6nS delay. At 25 MHz reference rate = 40 nS period 6-7 cards would be the cards per clock period. The targeted chassis has 10 cards in parallel for 9 delays and approximately 54 nS between the master and last slave (worst case). 54 nS is 1-2 clock periods. The clock and start pulse follow the same path and have the same worst case delays. The clock and trigger utilize two halves of dual driver and receiver pairs with low skew figures. The trigger is 2 periods wide to prevent the skew from causing a missed start.

The channels can be started with less skew between them by using an external clock and trigger distribution instead of the buffer/repeater network that is built into the cards.

DMA Xilinx Status

0x434

Bit#	Definition
0	DN01
2	DN45
4	DNL0
5	DNL1
6	DNA0
7	DNA1

DNx are the done bits from the Xilinx devices. After initialization the Done signal should be '1'.

DMA FIFO Holding Register Target Write

0x438

Bit#	Definition
31-0	Input FIFO data

Write data stored to the Input FIFO. Select the Input FIFO to write with the Channel definition. Enable the process with WRITE_EN_STD. The data is automatically written when a write to the holding register is detected. The hardware overlaps the write to the register and update of the FIFO to reduce the access time from the PCI bus.

DMA Status

0x43C

Bit#	Definition
0	Done channel 0
4	Done channel 4
8	FIFO_0_Err
9	FIFO_1_Err
10	gnd
11	gnd
12	gnd
13	gnd
14	gnd
15	Interrupt RQST
23-16	SW7-0
24	gnd
25	gnd
26	mt_out0n
27	hf_out0n
28	ff_out0n
29	mt_out1n
30	hf_out1n
31	ff_out1n

mt_xn is active low – '0' -> FIFO is empty
hf_xn is active low – '0' -> FIFO is half full or more
ff_xn is active low – '0' -> FIFO is full

x=0 corresponds to channel 0, and x=1 to channel 4.

Done channel x when '1' means that the requested samples have been transferred; i.e. the Data has been captured and stored into SDRAM, or read from SDRAM to the output FIFO as programmed. The done bits are cleared by writing a '1' to the corresponding position. The done bits are used to create an interrupt to the host if the corresponding interrupt enable bit is set. The bits should be cleared after the Xilinx's are enabled from reset to clear any transition induced status changes.

FIFO_X_Err when '1' indicates that the Output FIFO for that channel has become full at some point. In Transmit mode this is not a problem. In Direct mode this is an overflow error. Clear by writing with the corresponding bit set to '1'.

Interrupt RQST when '1' indicates that an enabled interrupt condition has occurred. In order to cause a system interrupt both the PLX interrupt enable and the INTERRUPT_MASTER_ENABLE in the base control register must be asserted.

SW7-0 reflects the settings of the user defined dip-switch on the board. It is envisioned that the switch is used as a board level "address" to identify a specific slot and cable with a particular device number.

DMA FIFO Holding Register DMA Write

0x2xxx

Bit#	Definition
31-0	Input FIFO data

To perform a write DMA, first select the Input FIFO to write to with the Channel definition, then enable the process by asserting WRITE_EN_DMA. When enabled and a write to this address occurs the DMA engine within the Xilinx is started. The data is written into the holding register, and then moved to the FIFO. An additional latch is used to create a three-deep pipeline. The initial READY signal is held off until the pipeline is ready for continuous data. The data within the register is updated on each clock until the BLASTn signal is asserted by the PLX device. BLASTn will be asserted when the Burst transfer from the PCI bus is halted due to length of transfer or software intervention. The PLX device requires about 6 clocks to arbitrate for the bus and start the transfer. The max time permitted for a transfer is 256 clocks leaving about 250 data transfers per burst. The transfer is interrupted with the BLASTn signal. The 2T design completes the writes of the data left in the pipeline when BLASTn is detected. The pipeline can handle 1, 2, 3+ length bursts. During this process the software should not attempt to access the PCI_LVDS_2T.

Address Generator Definitions

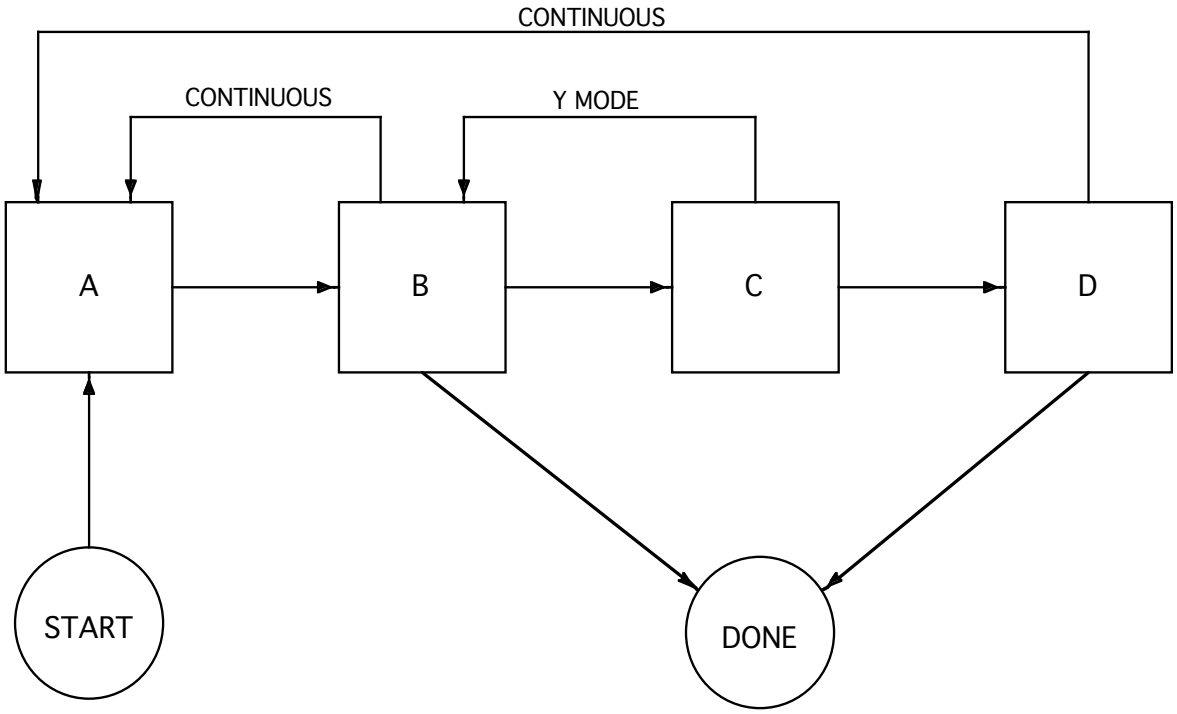

FIGURE 4 PCI_LVDS_2T ADDRESS GENERATOR ADDRESS LOOP OPTIONS

A, B, C and D represent the Address Generator registers A-D. Each register is available for each channel. The Address generator can be programmed to sequence: (1) from A to B and stop; (2) from A to B and then loop starting at A again; (3) from A to B the loop from B to C “Y” times, then progress to D; (4) same as 3 but loop from D to A. The following register definitions provide the programming details.

Address Generator SDRAM Address A Registers

0x080 ADD0_3 ADD CH 0 A
0x180 ADD4_7 ADD CH 4 A
Read – Write

Bit#	Definition
31	Start
30	Continuous
29	Y Count En
28	Store/transmit
27	Direct
26 - 25	unused / undefined
24-0	Initial address to access SDRAM for Channel

Two registers at different offsets with the same bit definitions provided for the 0, 4 channels.

The Address A register is the address to start with for accessing SDRAM. The SDRAM is organized as 64-bit words. The addresses increment with groups of 8 bytes. To select offset 8M bytes the address would be 1M 64-bit words. With a range of 24-0 the entire 256 Mbyte address space is selectable by any channel. All transfers will start and stop on 64-bit boundaries (by hardware definition). In no case are smaller than 64-bit data words written to or read from the SDRAM.

Start when '1' causes that channel to start-up. Only channel 0 or 4 can be used for Store, and any one channel can be used for Direct mode.

Continuous when set ('1') for a channel causes the channel to re-start at the end of the programmed sequence. When '0' the done bit will be set and the programmed operation stop at the end of the sequence. If started with the continuous bit set and later the bit is cleared then the process will terminate at the end of the current sequence.

Y Count En when '1' causes the hardware to use the Y count for that channel and to loop from address B to C – Y times.

Store/transmit when '1' selects store mode, when '0' selects transmit mode.

Direct when '1' selects the direct mode of transmission where data is moved directly from the input FIFO to the output FIFO bypassing the SDRAM.

With Y Count En = '1' the address will sequence from A to B then to C. From C, if the Y count is not at the terminal count then the next address will be B. When

the terminal count is reached the process will continue on to D. At D if the continuous bit is set the next address will be A. If the continuous bit is not set then the process is complete and the start bit will be cleared and the done bit set.

With Y Count En = '0' the start address is A and the stop address is B. With the continuous bit set the sequence will repeat.

There are no restrictions for page boundaries of the SDRAM. If the initial starting address is placed just before an SDRAM page boundary, then the hardware will process the first part of the transfer as a sequence of individual transfers then go to burst mode at the page boundary. If the length causes the address to cross a page boundary then the pipeline will detect this and stop prior to the page boundary, insert the proper control cycles and restart the burst on the next page. The hardware can handle the different combinations of starting, finishing, and crossing addresses automatically and at full rate as defined in the specification. If attempting to operate outside of the specification, then pay attention to the boundary conditions to increase performance. Pages are 0x00-0x3ff.

Any combination of channels can be activated for transmit mode. Only Channel 0 or 4 can be used for Store and any one channel can be used for **Direct** mode. The channels on the Address Generator should be activated before the corresponding channels on the Transmit Xilinx are set to transmit mode to make sure that there is data stored in the output FIFO.

The **Store** command must be started before the DMA sequence is initialized for loading data into SDRAM.

Address Generator SDRAM Address B Registers

0x090 ADD0_3 ADD CH 0 B
0x190 ADD4_7 ADD CH 4 B
Read – Write

Bit#	Definition
31	Initialization – Channel 0,4 B only
30	Load Complete – Channel 0,4 B only
29-28	unused / undefined
27	FF – read only FIFO Full Status
26	HF – read only FIFO Half Full Status
25	MT – read only FIFO Empty Status
24-0	Address Channel X register B definition

Two registers at different offsets with the same bit definitions provided for the 0, 4 channels.

The FIFO status bits are active low and read only.

The B register address is only for the termination or loop restart address depending on the Y Count En control bit. The Address is included in the transmission when used as a terminal address. Addresses are in 64-bit words.

The SDRAM requires initialization. The initialization involves a pre-charge cycle followed by a register write and then two refresh cycles. The hardware will stay in the low power undefined state until the initialization bit is set high. The SDRAM has an internal register which is controlled by writing to it with the "data" placed on the address lines. Channel 0, 4 Register A has been selected as the initialization source for the "data". **Prior to setting the initialization bit the data 0x27 must be written into the CH 0, 4 A register**. During the initialization cycle the 0x27 will be transferred to the SDRAM to set the CAS delay to 2 cycles and the burst size to page size. The hardware automatically will do the pre-charge, register write and refresh cycles. Once the initialization bit is set the software should delay for 2 uS before setting the channel 0 address to correspond to the channel 0 definition. The other channels can be set earlier because they are not involved with initialization. A further delay of 100 uS is required before using the SDRAM to allow for proper initialization.
After initialization the hardware enters a series of states called init_refresh where the SDRAM is ready to go but a command has not been detected. A counter delays for 256 clocks then a refresh occurs in an endless loop. When a command (start) has been set then the hardware will begin processing that command.

Load Complete (LC) when set tells the Store state-machine that the last of the data to transfer from the Input FIFO to the SDRAM is available. The state-machine will ignore the state of the HF flag and read the remaining data to complete the data Store operation. This bit is used once the DMA has completed the transfer from host memory into the PCI_LVDS_2T. The data at the end of the transfer will be stuck in the FIFO because the state-machine will not transfer data until there is at least 1/2 FIFO to transfer. The last 1/2 FIFO or less will be transferred as a final burst when the LC bit is set. This bit is not self cleared.

Address Generator SDRAM Address C Registers

0x0A0 ADD0_3 ADD CH 0 C
0x1A0 ADD4_7 ADD CH 4 C
Read – Write

Bit#	Definition
31-25	Y Count
24-0	Address C definition channel X

Two registers at different offsets 0, 4 channels.

The Address C definition is used when the Y Count En = '1'. The address represents the terminal address for the loop B-> C. The loop operates up to and including address C. In loop mode the next address after C will be B or C+1 if the loop is completed and the sequence is progressing toward D.

The Y count is the upper 7 bits of the C Address Register. The Count is tested at Address C when the Y Count En = '1'. If Y Count En = '0' the process stops at B with the loop count, and registers C and D ignored. The count range is 1-7F. The loop counts at B and tests at C. A '0' value would be 128 loops. If the continuous bit is set then the Y loop is repeated Y count times each time the main loop is repeated; indefinitely, stopped when the Start bit is cleared or the continuous bit is cleared at the end of the process.

Address Generator SDRAM Address D Registers

0x0B0 ADD0_3 ADD CH 0 D
0x1B0 ADD4_7 ADD CH 4 D
Read – Write

Bit#	Definition
24-0	Address D definition channel X

Two registers at different offsets 0, 4 channels.

The Address D definition is used when the Y Count En = ‘1’. The address represents the terminal address for the process. The loop operates up to and including address D. In Continuous mode the next address after D is A. In standard mode the start bit is reset and the done bit is set once D is reached on a per channel basis.

TX Definitions

TX CNTL_STAT Definition Registers

0x000 TX01 CNTL_STAT_0
0x100 TX45 CNTL_STAT_4
Read – Write

Two registers at different offsets 0, 4 channels.

Bit#	Definition
0	Start
1	Restart
2	Repeat Mode En
3	Serializer Enable
4	E1 Enable
5	E2 Enable
6	Read-Back mode
7	clock select
8	error – read only status bit
9	done – read only status bit

Serializer enable: When '0' the serializer is in power-down mode; when '1' the serializer is enabled. The serializer should be enabled with the idle pattern for 10 mS before starting a data transfer to allow the PLL to properly synchronize with the reference clock selected.

Start when '1' will start the transmitter sending data. The process assumes that the Address generator has been started before so that data is available in the Output FIFO. The process will continue until the done bit is received from the Address Generator and the FIFO becomes empty. If the FIFO is empty before the done bit is received the error flag is set. The Idle Pattern 0 is transmitted until the Start bit is set. Once set the pattern will become the data pattern until the end of the transmission. At the end of the transmission the second Idle Pattern will be transmitted.

Repeat Mode En when '1' enables the TX chip to interpret the upper data bits and to insert extra data based on the value found. The data is repeated for a programmed number of times (W, X, Y and Z registers contain the counts).
Bits 23, 22
00 W
01 X

10 Y
11 Z

The data is repeated for the programmed count on a per word basis. When Repeat Mode En = '0' the upper bits are ignored.

The Local Start and Master Start (from DMA Xilinx) are always used to transmit. In addition the E1 or E2 external enables can be required. When **E1 Enable** = '1' then the transmitter for that channel will not transmit until Start, Master and E1 are all set. Similarly if **E2 enable** is set then the transmission is held off until the E2 external enable is received. If both bits are '0' then the Master or Local Start will control when data is transmitted.

Read-Back Mode is selected to be able to read data from the FIFO to the internal control bus for data loop-back testing purposes.

The **Clock select** is used to select the reference clock to be the PCI clock or the muxed external or local reference clocks. See DMA Xilinx for more details on clock selection for operational modes. The PCI clock should be selected for the data loop-back mode.

The **Error bit** will be set and held when various error conditions occur.

The **Done bit** is a transitory bit and is only useful for factory test.

TX W Registers

0x008 W_COUNT_0
0x108 W_COUNT_4
Read – write
7 – 0 set the number of times to repeat data marked W.

TX X Registers

0x00C X_COUNT_0
0x10C X_COUNT_4
Read – write
7 – 0 set the number of times to repeat data marked X.

TX Y Registers

0x010 Y_COUNT_0
0x110 Y_COUNT_4
Read – write
7 – 0 set the number of times to repeat data marked Y.

TX Z Registers

0x014 Z_COUNT_0
0x114 Z_COUNT_4
Read – write
7 – 0 set the number of times to repeat data marked Z.

TX Idle 0 Registers

0x018 IDLE_0_0
0x118 IDLE_0_4
Read – write
20 – 0 Initial pattern to send while waiting for Start.

TX Idle 1 Registers

0x018 IDLE_1_0
0x118 IDLE_1_4
Read – write
20 – 0 Pattern to send upon completion of data transmission.

TX Data Read-back

0x004 DATA_RDBK_0
0x104 DATA_RDBK_4
Read only
31 – 0 Data from Output FIFO read for loop-back testing purposes.
Please note that once read the data is removed from the FIFO and needs to be reloaded before transmission can occur.

Operational Brief:

Data can be loaded into the local memory (2 x 256 MB SDRAM) via DMA or single write transfers (Store). Once the data is transferred the hardware is configured for transmission (Transmit). The appropriate channels are enabled and configured for synchronization options. The designated trigger event occurs and the data is transferred from SDRAM to the output serial channels.

In **Store** mode the data is input from the PCI bus and written to the SDRAM. The data can be input by single word writes from the host or by DMA programmed by the host and executed by the on-board DMA engine. The 9054 provides the PCI interface and DMA engine. The DMA Xilinx supports the DMA transfers by managing the input FIFO. The DMA transfers data from the PCI bus based memory to the Input FIFO. The Address Generator monitors the FIFO flags and when sufficient data is present bursts the data into memory. The data transfer from FIFO to SDRAM operates at 66 MHz and the PCI bus bursts at 33 MHz. The PCI_LVDS_2T can handle continuous input data bursts. The Half full flag is used to manage the bursts to the SDRAM. The Address Generator in conjunction with the DMA Xilinx switches from burst to single word transfers when there is less then 1/2 FIFO to read and the data has been completely transferred from the PCI memory into the Input FIFO. Any LW bounded length can be transferred into the Input FIFO. Any quad-word bounded length can be transferred into the SDRAM. In the case of a mis-match the data is repeated to fill the last location. Channel 0 and channel 4 are used to control the SDRAM data filling.

In **Transmit** mode the Address Generator works with the TX Xilinx to move data from SDRAM to the serializers. The software configures the Address Generator to enable the appropriate channels and initialize the initial pointer(s) and modes. The TX is also initialized for mode. The Address Generator when started will immediately fill the output FIFO for each enabled channel, then go into a round-robin arbitration mode to determine when to move additional data. The TX channels will wait until the programmed trigger event occurs then move data to the serializers. As soon as the TX channels have read enough data to cause the half-full flags to indicate not half-full the Address Generator will move another burst of data to that channel. The Address Generator will continue to operate until all enabled channels have completed. Normally all of the channels are in the same mode, but they do not have to be. All channels that are enabled have to be in Transmit mode. Within Transmit mode the channels are independent for the looping options.

In **Direct** mode the data is moved from the Input FIFO to the Output FIFO

bypassing the SDRAM. The half-full flags are used to determine when there is data in the input side and room in the output side. The output clock rate and expansion factor determine the rate data is read from the Output FIFO. The PCI bus activity will determine if the input data can keep pace with the output. With no expansion the PCI side has an advantage over the output side at max transmission rate.

The Hardware should be initialized Address generator first, TX second, DMA third, PLX last. The PLX chip can be initialized all but the last step of enabling the DMA function before doing the Xilinx definitions. Once the PLX is started the data can begin to flow through the board. In Direct mode The PLX will start to fill the Input FIFO. When the FIFO is half full the Address Generator will start to transfer from the Input FIFO to the Output FIFO for the channel that is enabled. The TX will sense that there is data in the Output FIFO and begin the transmission (should already be enabled in this mode). The DMA Xilinx will sense that there is room in the Input FIFO as soon as the Address Generator has read below the half-full point and start another DMA from host memory. The Address Generator will attempt to keep the Output FIFO close to Full by loading 1/2 FIFO each time the FIFO has 1/2 FIFO available. The DMA Xilinx will attempt to keep the Input FIFO full by loading via DMA 1/2 FIFO each time the Input FIFO is less than 1/2 full. The PCI bus has more than the base bandwidth of the output data stream. As long as the PCI bus is available, without delay, the Direct mode can function without gaps in the output data stream. If any of the TX expansion factors are used the leverage of the PCI bus over the transmission rate increases making the “job” easier.

The PLX device should be programmed to start the DMA transfer. The PLX will then start-up when commanded, wait for the DMA Xilinx to respond (FIFO is less than half full on programmed channel and state-machine has started up) then request the PCI bus. The Bus arbitration and start-up take 6 clocks. Assuming that the PCI bus is not busy delaying the start of the burst, the DMA Xilinx and the PCI bus will be synchronized and data will flow from the PCI Bus to the Input FIFO. If the PCI bus has an issue or the max time has expired the PLX device will issue a BLASTn signal to the DMA Xilinx to halt the transfer. When there is room within the PLX FIFO the process will restart. The pipeline will retain the previous state and begin again where it left off. If the PCI bus is not used by other devices the only down time will be the 6 clocks for arbitration plus an additional 3 within the DMA Xilinx to restart. Theoretical maximum is 250 data samples per 250+9 clocks for a maximum bandwidth of 127.4 Mbytes/Sec. The SDRAM can support this data-rate in Store mode. The Direct mode will be restricted by the samples gathered and the clock rate of the Output data stream.

LVDS Connector Definition

(3M N102A0-52E2VC)

Pin	Signal Name	Alternate Name
1	GND*	
2	ECLKINP	
3	ECLKINM	
4	ETRIGINP	
5	ETRIGINM	
6 – 9	SPARE	
10	CH6TXCLKP	06_CLK_T
11	CH6TXCLKM	06_CLK_C
12	CH6TX2P	
13	CH6TX2M	
14	CH6TX1P	06_UDATA_T
15	CH6TX1M	06_UDATA_C
16	CH6TX0P	06_LDATA_T
17	CH6TX0M	06_LDATA_C
18	GND*	
19	GND*	
20	CH4TXCLKP	04_CLK_T
21	CH4TXCLKM	04_CLK_C
22	CH4TX2P	
23	CH4TX2M	
24	CH4TX1P	04_UDATA_T
25	CH4TX1M	04_UDATA_C
26	CH4TX0P	04_LDATA_T
27	CH4TX0M	04_LDATA_C
28	GND*	
29	GND*	
30	CH1TXCLKP	01_CLK_T
31	CH1TXCLKM	01_CLK_C
32	GND*	
33	CH1TX2P	
34	CH1TX2M	
35	CH1TX1P	01_UDATA_T
36	CH1TX1M	01_UDATA_C
37	CH1TX0P	01_LDATA_T
38	CH1TX0M	01_LDATA_C
39	GND*	
40	GND*	
41	CH0TXCLKP	00_CLK_T

42	CH0TXCLKM	00_CLK_C
43	CH0TX2P	
44	CH0TX2M	
45	CH0TX1P	00_UDATA_T
46	CH0TX1M	00_UDATA_C
47	CH0TX0P	00_LDATA_T
48	CH0TX0M	00_LDATA_C
49	GND*	
50	GND*	
51	ECLKOUTP	
52	ECLKOUTM	
53	ETRIGOUTP	
54	ETRIGOUTM	
55 – 60	SPARE	
61	CH7TX0M	07_LDATA_C
62	CH7TX0P	07_LDATA_T
63	CH7TX1M	07_UDATA_C
64	CH7TX1P	07_UDATA_T
65	GND*	
66	CH7TX2M	
67	CH7TX2P	
68	CH7TXCLKM	07_CLK_C
69	CH7TXCLKP	07_CLK_T
70	GND*	
71	GND*	
72	CH5TX0M	05_LDATA_C
73	CH5TX0P	05_LDATA_T
74	CH5TX1M	05_UDATA_C
75	CH5TX1P	05_UDATA_T
76	CH5TX2M	
77	CH5TX2P	
78	CH5TXCLKM	05_CLK_C
79	CH5TXCLKP	05_CLK_T
80	GND*	
81	GND*	
82	CH3TX0M	03_LDATA_C
83	CH3TX0P	03_LDATA_T
84	CH3TX1M	03_UDATA_C
85	CH3TX1P	03_UDATA_T
86	CH3TX2M	
87	CH3TX2P	
88	CH3TXCLKM	03_CLK_C
89	CH3TXCLKP	03_CLK_T

90	GND*	
91	GND*	
92	CH2TX0M	02_LDATA_C
93	CH2TX0P	02_LDATA_T
94	CH2TX1M	02_UDATA_C
95	CH2TX1P	02_UDATA_T
96	CH2TX2M	
97	CH2TX2P	
98	CH2TXCLKM	02_CLK_C
99	CH2TXCLKP	02_CLK_T
100	GND*	

GND* = AC, DC, Open connection to Ground. Standard = open.

Construction and Reliability

PCI Modules were conceived and engineered for rugged industrial environments. The PCI_LVDS_2T is constructed out of 0.062 inch thick FR4 material. The connector bezel and extender bracket provide support at both ends of the card in addition to the PCI connector.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components.

Thermal Considerations

The PCI_LVDS_2R design consists of CMOS circuits. The power dissipation due to internal circuitry other than the SDRAM is very low. Forced air cooling is recommended. Commercial temperature components are utilized. 0-70 C is the case temperature range for these components. Sufficient forced air is required to provide adequate cooling to keep the component temperatures within normal operating limits. In most chassis very minimal air flow will be required. The airflow required will be a function of the temperature of the cooling air, and the amount of heat to dissipate from the PCI_LVDS_2R and the other cards installed into the same chassis.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

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Dynamic Engineering

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