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User Manual

PC104p-BiSerial-BAE2

UART and Parallel Port

PC/104p Module

Revision A1
Corresponding Hardware: Revision A
10-2004-0601

PC104p-BiSerial-BAE2
Bi-Directional Serial Data
Interface
PC/104p Module

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Product Description

The PC104p-BiSerial-BAE2 is part of the PC/104p Module family of modular I/O components by Dynamic Engineering. The PC/104p-BiSerial is capable of providing multiple serial protocols. The BAE2 protocol implemented provides an RS-422 UART and parallel port capability. The BAE2 version is minimized and does not include the ADC, DAC, PLL, TTL or external FIFOs.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a "standard" special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

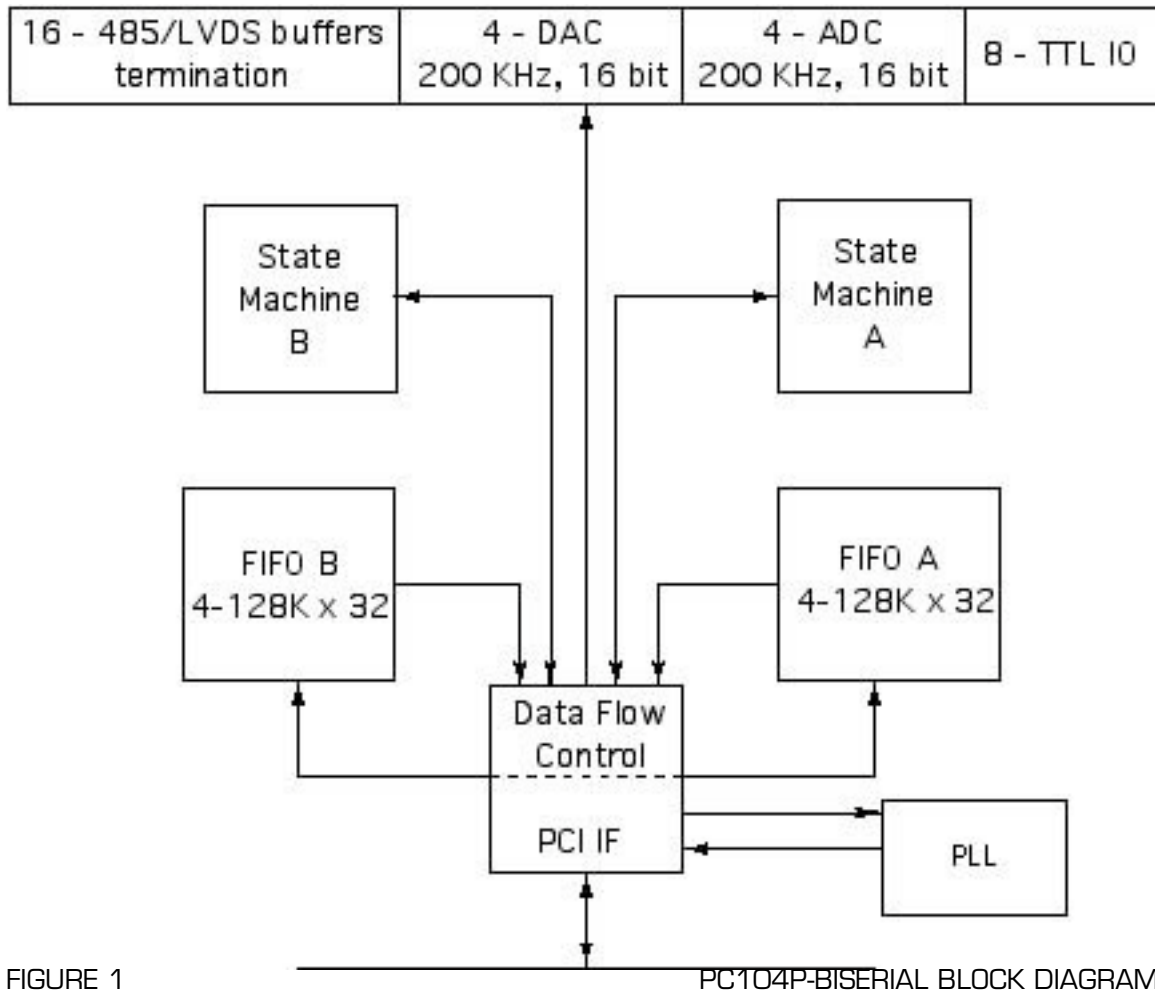


FIGURE 1

PC104P-BISERIAL BLOCK DIAGRAM

The standard configuration shown in Figure one makes use of two external [to the Xilinx] FIFOs. The FIFOs can be as large as 128K deep x 32 bits wide. Some

designs do not require so much memory and are more efficiently implemented using the internal FIFOs. Internal FIFOs can be configured using the block RAM within the Xilinx.

Sixteen differential I/O are provided for the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 100Ω . The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pullup/pulldown resistor packs can also be installed to provide a logic '1' on undriven lines.

The terminations and transceivers are programmable through the Xilinx device to provide the proper mix of outputs, inputs and terminations needed for a specific protocol implementation. The Serial interface uses two of the 16 differential IO. All 16 bits can be programmed to be Parallel data or the alternate function – UART data or ground via the source control register. The terminations are programmable for all IO.

All configuration registers support read and write operations for maximum software convenience, and all addresses are long word aligned.

The PC104p-BiSerial conforms to the PC/104p standard. This guarantees compatibility with multiple PC/104p boards. Because the PC/104p may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCI2PC104p – PCI carrier for PC/104p can be used for development in a conventional PC. Later the hardware and software can be ported to the target.

The serial format for transmit and receive is UART. The electrical format is RS422. Data is high for frame, low for the start bit, lsb first with programmable parity and programmable stops bits.

The baud rate is also programmable. The software selects the divisor to use. The base clock rate is 18.432 MHz from a reference oscillator.

Various interrupts are supported by the PC104p-BiSerial . An interrupt can be configured to occur at the end of a transmitted message. An interrupt can be set at the end of a reception. All interrupts are individually maskable and a master interrupt enable is also provided to disable all interrupts simultaneously.

Theory of Operation

The PC104p-BiSerial-BAE2 is designed for transferring data from one point to another with a simple serial protocol.

The PC104p-BiSerial-BAE2 features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the PC104p-BiSerial design. Only the transceivers, and switches are external to the Xilinx device in this application.

The PCI interface to the host CPU is controlled by a logic block within the Xilinx. The PC104p-BiSerial design requires one wait state for read or write cycles to any address. The PC104p-BiSerial is capable of supporting 40 MBytes per second into and out of the FIFO's. The wait states refer to the number of clocks after the PCI core decode before the "terminate with data" state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate with data state into the TRDY signal.

The PC104p-BiSerial can support many protocols. The PC104p-BiSerial-BAE2 uses UART protocol.

State machines within the FPGA control all transfers between the internal registers and FPGA logic, and the FPGA and the data buffers. The TX state machine reads from the transmit data register and loads the shift register before sending the data. The RX state machine receives data from the data buffers and takes care of moving data from the shift register into the RX storage.

Data is read from the TX register and loaded into the shift register. The LSB is then present at the output of the data buffer. One bit period later the data is transitioned to the next value. The LSB+1 is now on the data lines. This process repeats until the first word is transferred. If more data is available, then the process repeats for the second character. In the standard timing there are programmable "stop bit" gaps. Please refer to the register bit definitions for more details.

The data rate is set by a 9-bit field in the control register. The reference clock is divided by the value in the count to create the output rate. The UART protocol requires that the data is in the marking state or stop state before a new character is sent. The first bit sent is the start bit ['0'] followed by the 8 data [LSB first], then parity [programmable odd, even, none], and the stop bit(s). The transceivers are rated for 40 MHz. The interface is asynchronous and the receiver requires some margin 16x to be able to accurately determine the bit boundaries and to decode the data correctly.

The receive function uses a free running shift register coupled with the receive state-machine to capture the data. The data is sampled and when the start bit is detected, synchronizes to the received data stream. The data bits are extracted and tested for parity. The stop bits are tested to check the frame size.



If the receiver is enabled and a transmission is already in progress, the receiver will ignore the data until the data is determined to be in a marking state to insure that the lead 0 is a start bit not a character bit.

Address Map

PC104P_BIS_BASE	0x0000 // 0	base control register offset
PC104P_BIS_IER	0x0004 // 1	Int Enable control register offset
PC104P_BIS_UART_CNTL	0x0010 // 4	UART control register offset
PC104P_BIS_STAT1	0x0018 // 6	status register switch, revision
PC104P_INT_STAT	0x001C // 7	Int control and status register offset
PC104P_BIS_DIR_TERM	0x0028 // 10	direction and termination register
PC104P_BIS_PARDAT_485	0x002C // 11	parallel 485 data output register
PC104P_BIS_PARCNTL	0x0030 // 12	parallel data control register
PC104P_BIS_UART0	0x003C // 15	UART data register offset

FIGURE 2

PC/104P-BISERIAL-BAE2 ADDRESS MAP

The address map provided is for the local decoding performed within the PC104p-BiSerial-BAE2. The addresses are all offsets from a base address, which is assigned by the system when the PCI bus is configured.

The VendorId = 0x10EE. The CardId = 0x001E. Current revision = 0x00

Programming

Programming the PC104p-BiSerial-BAE2 requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PC104p-BiSerial-BAE2 "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to receive data the software is only required to enable the receiver, and set the expected protocol definitions. To transmit the software will need to load the character into the output buffer, set the frequency, protocol variables, and enable the transmitter.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the UART interrupts. After the interrupt is received, the data can be retrieved or a new character sent.

The TX interrupt indicates to the software that a character is being sent and that the hardware can handle a new one. If more than one interrupt is enabled, then the SW needs to read BIS2_STAT1 to see which source caused the interrupt. The status bits of BIS2_STAT1 are latched and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definition

Register Definitions

PC104P_BIS_BASE

[\$00] PC104p-BiSerial Base Control Register Port read/write

BASE Control Register	
DATA BIT	DESCRIPTION
31-11	Spare
10	Alt SW1
9	Alt SW0
8	Mux Control
7-0	spare

FIGURE 3

PC104P-BISERIAL-BAE2 BASE CONTROL REGISTER BIT MAP

When Mux Control = '0' [default] the external switch controls the select lines to the external mux. The external Mux controls which clock, IDSEL and interrupt to use. When Mux Control is set to '1' the bits 10,9 are used instead of the switch to control the mux. 00 corresponds to slot 0 01 to slot 1 etc.

PC104P_BIS_IER

[\$04] PC104p-BiSerial Interrupt Control Register Port read/write

Interrupt Enable Register	
DATA BIT	DESCRIPTION
31-18	Spare
17	Master Interrupt Enable
16	Interrupt Set
15-8	spare
7	UART Parity Error INT EN
6	UART Frame Error INT EN
5	UART Data Available INT EN
4	UART TX Done INT EN
3-0	spare

FIGURE 4

PC104P-BISERIAL-BAE2 IER REGISTER BIT MAP

Master Interrupt Enable when '1' allows interrupts generated by the PMC-BiSerial-II-PS2 to be driven onto the backplane [INTA]. When '0' the interrupts can be individually enabled and used for status without driving the backplane. Polled operation can be performed in this mode.

Interrupt Set when '1' and the Master is enabled, forces an interrupt request. This feature is useful for testing and software development.

UART TX done when '1' enables an interrupt when the transmitter is ready for the next character.

UART Data Available when '1' enables an interrupt when the receiver has data to read.

UART Frame Error when '1' enables an interrupt when a Frame error is detected

UART Parity Error when '1' enables an interrupt when a Parity Error is detected.

PC104P_BIS_UART_CNTL

[\$10] PC104p-BiSerial-BAE2 UART control Port read/write

UART Control	
DATA BIT	DESCRIPTION
31-13	Spare
12-4	baud rate selector
3	stop
2	parity
1	parity enable
0	enable

FIGURE 5

PC104P-BISERIAL-BAE2 UART CONTROL REGISTER BIT MAP

Enable when '1' enables the UART to transmit and to receive characters. The UART will automatically transmit when a character is loaded into the holding register.

Parity enable when '1' causes parity to be inserted into the data stream and for parity to be checked on the incoming signal.

Parity when '1' selects odd parity and when '0' even parity. Note that parity enable must be '1' for this bit to be applied to the data.

Stop when '0' puts 1 stop bit at the end of the character sent. Stop when '1' puts 2 stop bits at the end of the message. If there is more data to send the stop bit(s) is/are immediately followed by the next start bit. If there is no more data to send then marking bits are sent until there is data to send.

PC104P_BIS_STAT1

[\$18] PC104p-BiSerial-BAE2 Status Port read only

Switch and Revision Port	
DATA BIT	DESCRIPTION
31-16	Spare
15-12	revision
11-8	Model
7-2	spare
1-0	switch in

FIGURE 6

PC104P-BISERIAL-BAE2 STATUS BIT MAP

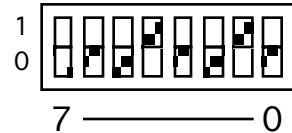
The dip switch can be read with the lower two bits of this port. Direct mapping.

The model for the BAE2 version is 0x1.

The revision is 0x1.

The Switch Read Port has the user bits. The user bits are connected to the eight dip-switch positions. The switches allow custom configurations to be defined by the user and for the software to identify a particular board by its switch settings and to configure it accordingly.

The Dip-switch is marked on the silk-screen with the positions of the digits and the '1' and '0' definitions. The numbers are hex coded. The example shown would produce 0x12 when read. On the rev A fab only the lowest 2 bits are in use.



PC104P_INT_STAT

[\$1C] PC104p-BiSerial-BAE2 Interrupt Status Port read/write

CONTROL		RX
DATA	BIT	DESCRIPTION
31-8		Spare
7		UART PAR
6		UART FRM
5		UART DAV
4		UART DN
3-0		spare

FIGURE 7 PC104P-BISERIAL-BAE2 INTERRUPT STATUS BIT MAP

When set the bit indicates a pending interrupt source. If the master interrupt is enabled and the bit interrupt is enabled then an interrupt will be driven onto INTA. If the master is not enabled or if the particular bit is not enabled then the status will still be set, but the interrupt will not occur. Unused bits should be masked off to avoid confusion.

UART DN when '1' indicates that the TX is ready for a new character. Please note that the very first character will create an interrupt at the end of the character being sent. Your software will send the first character then use the interrupt to know when to send the second ...etc.

UART DAV when '1' indicates that there is data available to be read from the receiver.

UART FRM when '1' indicates that a FRAME Error has occurred.

UART PAR when '1' indicates that a PARITY Error has occurred.

The status bits are cleared by writing a '1' back to that bit position. The clear happens during the write so there is no need to write again with '0' to "clear the clear". Multiple bits can be cleared with one write. After initialization and before use it is a good idea to clear any pending interrupts to make sure operating status is current.

PC104P_BIS_DIR_TERM

[\$28] PC104p-BiSerial-BAE2 Direction and Termination Register Port read/write

CONTROL DIR_TERM REGISTER			
DATA BIT	DESCRIPTION		
15-0	DIRection	15-0	0 = read 1 = drive
31-16	TERMination	15-0	1 = terminated

FIGURE 8 PC104P-BISERIAL-BAE2 DIRECTION TERMINATION CONTROL BIT MAP

The direction for each of the 16 differential pairs is controlled through this port. The port defaults to zero, which corresponds to tri-stating the drivers and no terminations enabled.

Pull-up and Pull-down resistors built into some '485 interface devices may make the signal appear to be driven (if open) when in the tri-stated mode. Enabling the termination on a tri-stated line will yield approximately 2.5V on each side of the tri-stated driver.

<u>CONTROL</u>	<u>CORRESPONDING IO BITS</u>
DIR_15-0	IO_15-0

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others it will make sense to use the onboard terminations.

The terminations for the receive groups should be set to terminate with the user software in most cases. If the Parallel Port is set to be an input with the direction bits then the corresponding termination bits should also be set.

<u>CONTROL</u>	<u>CORRESPONDING IO BIT(S)</u>
TERM_15.0	IO_15..0

PC104P_BIS_PARDAT_485

[\$2C] PC104p-BiSerial-BAE2 Parallel Data Output Register read/write

CONTROL UART	
DATA BIT	DESCRIPTION
31-16	Spare
15-0	parallel output data

FIGURE 9

PMC BISERIAL-II PARALLEL OUTPUT DATA BIT MAP

There are 16 potential output bits in the parallel port. The Direction and Termination register sets the direction of the bits. When the direction is set to output and the source control is set to parallel port then the bit definitions from this register are driven onto the corresponding parallel port lines.

This port is direct read-write of the register. The IO side is read-back from this port. It is possible that the output data does not match the IO data in the case of the Direction bits being set to input.

PC104P_BIS_PARCNTL

[\$30] PC104p-BiSerial-BAE2 Parallel Port Source Control Port

Parallel Port Control	
DATA BIT	DESCRIPTION
31-16	Spare
15-0	Parallel Port Source Definitions

FIGURE 10

PC104P-BISERIAL-BAE2 DATA SOURCE BIT MAP

Each of the Parallel Port bits has a corresponding source control bit. When the bit is set '1' the parallel data is used [PC104P_BIS_PARDAT_485]. When '0' the defined IO is used. The BAE2 design uses bit 0 for the UART TX and bit 8 for the UART RX channel. All other bits are set to '0' when not selected to be parallel bits. Please note that the direction control bit needs to be set to make the port bits act as inputs or outputs. For example the UART requires bit 0 to be set to output, to allow the transmitted bits to be transmitted. If used as a parallel port Bit 0 can be defined as input or output.

PC104P_BIS_UART0

[\$3C] PC104p-BiSerial-BAE2 UART Data Port Write Tx characters, Read Rx characters

UART DATA	
DATA BIT	DESCRIPTION
7-0	UART 7-0

FIGURE 11

PC104P-BISERIAL-BAE2 UART DATA BIT MAP

If the UART is enabled then writing to this port will cause a character to be transmitted. Please note that the direction bit needs to be set to transmit on IO bit 0, and the data source set to UART not parallel port. The data will be sent with the baud rate, parity and stop bit configuration in the UART control register. The control register should be set before using the port.

When data has been received and a character stored the data is read via this port. The port is read-write, and the data read is from the UART RX not the data holding register.

Interrupts

PC104p-BiSerial-BAE2 interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with a PC104p-BiSerial-BAE2 interrupt the software must read the status register to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

For example, the PC104p-BiSerial-BAE2 UART state machine generates an interrupt request when a transmission is complete and the Tx int enable and Master interrupt enable bits are set. The transmission is considered complete when the last bit is output from the output shift register.

The interrupt is mapped to INTA on the PC/104p connector, which is mapped to a system interrupt when the PCI bus configures. The source of the interrupt is obtained by reading the Interrupt Status register. The status remains valid until that bit in the status register is explicitly cleared.

When an interrupt occurs, the Master interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the latched bit and set the Master interrupt enable bit high again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the Interrupt Status register.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The BAE2 version of the PC104p-BiSerial-BAE2 utilizes a 50 pin right angle header connector. The test requires an external cable [ribbon] with the following pins connected. Upper Byte to Lower byte.

SIGNALs	+	-	+	-
I00/I08	1	2	17	18
I01/I09	3	4	19	20
I02/I010	5	6	21	22
I03/I011	7	8	23	24
I04/I012	9	10	25	26
I05/I013	11	12	27	28
I06/I014	13	14	29	30
I07/I015	15	16	31	32

PC104p-BiSerial-BAE2 Header Pin Assignment

The figure below gives the pin assignments for the header connector on the PC104p-BiSerial design. Please note that the Analog and TTL IO is not installed on this version. GND* is a plane which is tied to GND through a 0805 0Ω resistor. DC, AC or open are options. For customized version, or other options, contact Dynamic Engineering.

IO_0P [UART TX]	IO_0m	1	2
IO_1P	IO_1m	3	4
IO_2P	IO_2m	5	6
IO_3P	IO_3m	7	8
IO_4P	IO_4m	9	10
IO_5P	IO_5m	11	12
IO_6p	IO_6m	13	14
IO_7p	IO_7m	15	16
IO_8p [UART RX]	IO_8m	17	18
IO_9p	IO_9m	19	20
IO_10p	IO_10m	21	22
IO_11p	IO_11m	23	24
IO_12p	IO_12m	25	26
IO_13p	IO_13m	27	28
IO_14p	IO_14m	29	30
IO_15p	IO_15m	31	32
GND*	GND*	33	34
ADCO	TTL0	35	36
ADC1	TTL1	37	38
ADC2	TTL2	39	40
ADC3	TTL3	41	42
DACO	TTL4	43	44
DAC1	TTL5	45	46
DAC2	TTL6	47	48
DAC3	TTL7	49	50

FIGURE 12

PC104P-BISERIAL CONNECTOR PINOUT

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard ribbon cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC BiSerial-II when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The PMC BiSerial-II does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the BiSerial II pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68-screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68

[<http://www.dyneng.com/HDRterm50.html>]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages.



Construction and Reliability

PC/104p Modules were conceived and engineered for rugged industrial environments. The PC/104p-BiSerial is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PC/104p device is secured into the stack with high insertion force pins and four screws attached to the 4 stand-offs. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PC/104p Module provides a low temperature coefficient of $1.7 \text{ W}/^{\circ}\text{C}$ for uniform heat. This is based upon the temperature coefficient of the base FR4 material of $0.31 \text{ W}/\text{m}^{\circ}\text{C}$, and taking into account the thickness and area of the PC/104p. The coefficient means that if 1.7 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PC104p-BiSerial design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.



Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

<http://www.dyneng.com/warranty.html>

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is \$100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
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831-336-8891
831-336-3840 fax

support@dyneng.com



Specifications

Host Interface:	PC/104p - 32 bit PCI bus
Serial Interface:	16 bit RS422 parallel port with UART port.
Tx Data rates generated:	18.432 MHz reference with 9 bit baud rate selector
Rx Data rates accepted:	Up to 1.152 MHz..
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses
Interrupt:	UART interrupt at end of transmission UART when data available UART interrupt on receive error Software interrupt
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin ribbon cable or discrete wire 50 screw terminal block interface
Dimensions:	Standard Single PC/104p Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	1.7 W/°C for uniform heat across PC/104p
Power:	Max. TBD mA @ 5V



Order Information

PC104p-BiSerial-BAE2

PC/104p Module with RS422 UART and parallel port

Eng Kit

HDRterm50 - 50 position screw terminal adapter

<http://www.dyneng.com/HDRterm50.html>

HDEcabl68 - 68 IO twisted pair cable

<http://www.dyneng.com/HDRribn50.html>

Technical Documentation,

1. PC104p-BiSerial Schematic

2. PC104p-BiSerial-BAE2 Reference test software

Data sheet reprints are available from the manufacturer's web site

reference software: C source code requires WinRT.

Windows driver option.

Note: The Engineering Kit is strongly recommended for first time PC/104p-BiSerial purchases.

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.

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