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User Manual

IP-Pulse

4 Channel Digital Pulse Generator
IP Module

4 TTL /	0 422	- TTL
3 TTL /	1 422	–1
2 TTL /	2 422	–2
1 TTL /	3 422	–3
0 TTL /	4 422	-422

Manual Revision B
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IP Module

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Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Manual Revision B. Revised 5/17/05

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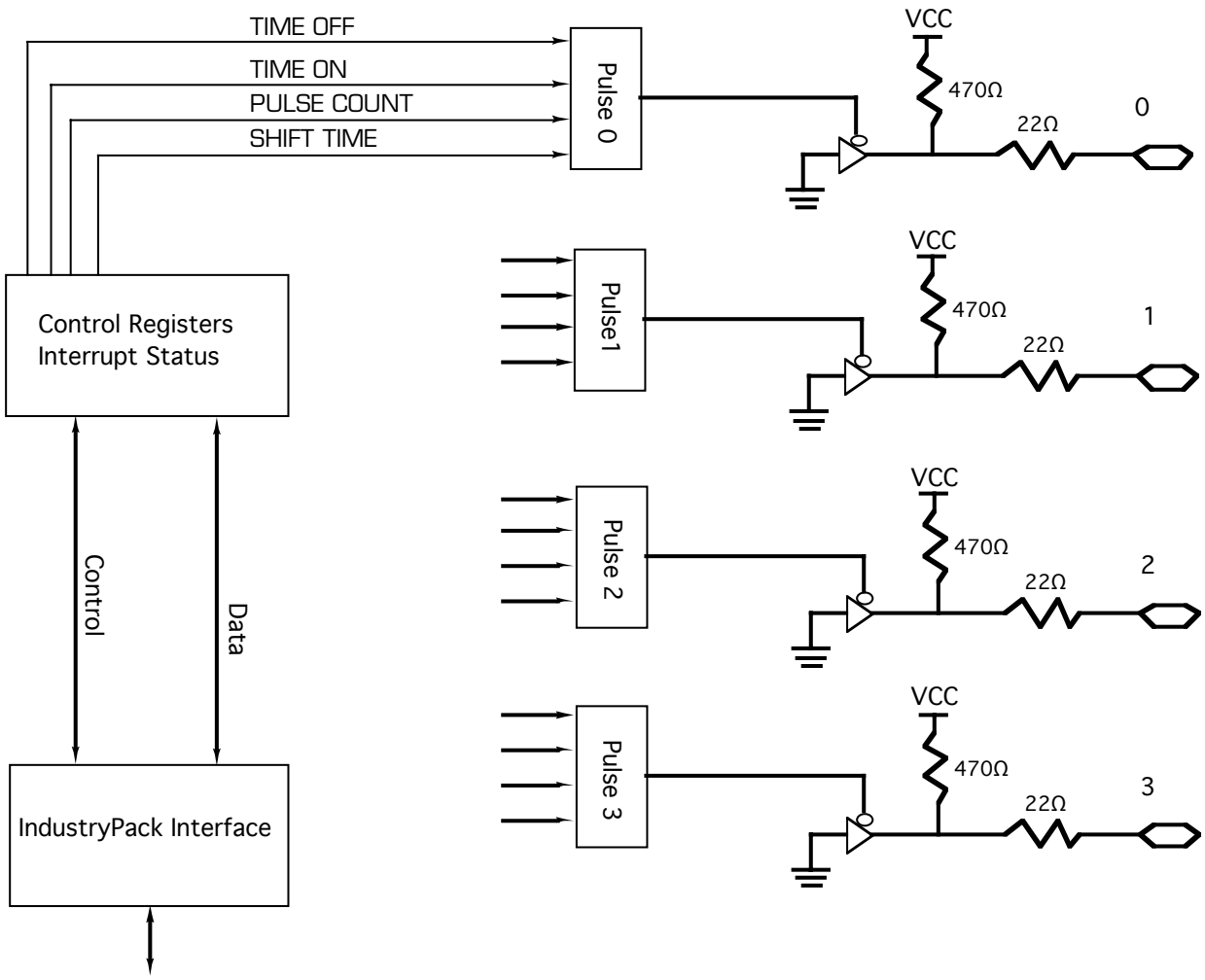
Product Description and Operation



IP-Pulse is part of the IP Module family of modular I/O components. IP-Pulse is designed to provide 4 independent programmable outputs. Each output can be initialized with time off, time on, inverted, number of pulses to generate, and interrupt per pulse. The reference is a 50 MHz oscillator that provides a 20 nS resolution to your programmed pulse.

The TTL version provides 4 TTL/CMOS level outputs. The 422 version has 4 RS422/485 compatible outputs. The mixed versions have some of each output type.

Each output has several registers associated with it; time off, time on, shift, and pulse control, The registers are more than 16 bits in width requiring two addresses per register.

The time off register contains the value for the time before the first pulse and the time between subsequent pulses. The time off does not include the time on.

The time on register contains the time that the pulse is asserted.

The Shift Register contains the amount of time to shift. When the Pulse Control Register is written to with the shift enable set, the time in the shift register is added to the current pulse off time. The enable is auto cleared after the shift enable is processed. The shift happens one time per valid request. Asking for a shift before the previous shift has been processed will be ignored. The shift feature can be used to create a phase offset between two pulse streams. The shift is always added. Two, three or 4 of the outputs can be coordinated to control phase dependent hardware or to simulate the input from a synchro etc.

The Pulse Control register contains the number of pulses to send ['0' = infinite] and control bits for interrupts, pulse inversion, shift, new ON time,, new OFF time, and a channel specific enable. The base register contains a master enable that can be used to synchronize the 4 outputs.

Interrupts can be generated if desired. The Master enable allows the use of polling if that is preferred. The pulse count completed condition, and pulse generated condition can be used as interrupt sources. If using the pulse generated condition an interrupt will be generated each time a pulse is transmitted. With longer periods this feature can help to keep your software in synchronization with your system. The interrupt feature can also be used as a programmable timer for your software to use if the output is not required.

The interrupts are individually maskable – each channel has a separate mask. The vector is user programmable by a read/write register. The interrupt occurs on IntReqO. The vector can be read in the IO space or automatically with the INT space. The use of the vector is not required by the IP-Pulse and is provided for systems that require the use of a vector.

In the versions with 485 transceivers the control bits have the same definitions. The IO connector pin definitions change. Please refer to the appropriate pinout table in the rear of this manual.

Custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there, we will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a "standard" special order product. Please contact Dynamic Engineering with your custom application. Several of the IO bits are implemented on the long line clock pins of the FPGA. External clock references can be designed in as a custom option. There is a user oscillator position to support custom state machines and IO requirements. The DMA controls, second interrupt level, and memory space controls are routed to the FPGA to allow for future upgrades.

The IP-PULSE supports both 8 and 32 Mhz. IP Bus operation. Most configuration registers support read and write operations for maximum software convenience. Word operations are supported (please refer to the memory map). The ID, IO, and INT spaces are utilized by the IP-Pulse design.

The IP-PULSE conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. The PCI3IP card makes a convenient development platform in many cases. http://www.dyneng.com/pci_3_ip.html

Address Map

Name		Offset	Width	Function
ip_parpls_base	EQU	$00	word	Base Control Register
ip_parpls_stat	EQU	$02	word	Status Register
ip_parpls_vector	EQU	$04	word	Interrupt Vector Register in IO space
ip_parpls_toff0_l	EQU	$10	word	Channel 0 OFF time lower
ip_parpls_toff0_u	EQU	$12	word	Channel 0 OFF time upper
ip_parpls_ton0_l	EQU	$14	word	Channel 0 On time lower
lip_parpls_ton0_u	EQU	$16	word	Channel 0 On time upper
ip_parpls_pccr0_l	EQU	$18	word	Channel 0 Pulse Control register lower
ip_parpls_pccr0_u	EQU	$1A	word	Channel 0 Pulse Control register upper
ip_parpls_shft0	EQU	$1C	word	shift count register channel 0
ip_parpls_toff1_l	EQU	$20	word	Channel 1 OFF time lower
ip_parpls_toff1_u	EQU	$22	word	Channel 1 OFF time upper
ip_parpls_ton1_l	EQU	$24	word	Channel 1 On time lower
lip_parpls_ton1_u	EQU	$26	word	Channel 1 On time upper
ip_parpls_pccr1_l	EQU	$28	word	Channel 1 Pulse Control register lower
ip_parpls_pccr1_u	EQU	$2A	word	Channel 1 Pulse Control register upper
ip_parpls_shft1	EQU	$2C	word	shift count register channel 1
ip_parpls_toff2_l	EQU	$30	word	Channel 2 OFF time lower
ip_parpls_toff2_u	EQU	$32	word	Channel 2 OFF time upper
ip_parpls_ton2_l	EQU	$34	word	Channel 2 On time lower
lip_parpls_ton2_u	EQU	$36	word	Channel 2 On time upper
ip_parpls_pccr2_l	EQU	$38	word	Channel 2 Pulse Control register lower
ip_parpls_pccr2_u	EQU	$3A	word	Channel 2 Pulse Control register upper
ip_parpls_shft2	EQU	$3C	word	shift count register channel 2
ip_parpls_toff3_l	EQU	$40	word	Channel 3 OFF time lower
ip_parpls_toff3_u	EQU	$42	word	Channel 3 OFF time upper
ip_parpls_ton3_l	EQU	$44	word	Channel 3 On time lower
lip_parpls_ton3_u	EQU	$46	word	Channel 3 On time upper
ip_parpls_pccr3_l	EQU	$48	word	Channel 3 Pulse Control register lower
ip_parpls_pccr3_u	EQU	$4A	word	Channel 3 Pulse Control register upper
ip_parpls_shft3	EQU	$4C	word	shift count register channel 3
Pulse_IDPROM			byte on word boundary	read

FIGURE 1 IP-PULSE INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within IP-PULSE. The addresses are all offsets from a base address. The carrier board that the IP is installed into provides the base address. Please note that the memory map has changed compared to the previous revisions. Revision D and newer PROMs use the above memory map. The new memory map has long word oriented register definitions to allow use in carriers with 32 bit capability – PCI3P, PCI5IP, cPCI2IP, and cPCI4IP for example. The Shift registers have been added and new control bits added to the Pulse Control registers.

Programming

Programming IP-PULSE requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Carrier board.

In order to transmit pulses; the off, on, and PCCR registers for the channel(s) of interest need to be initialized and then the master enable set. The off and on values represent the number of periods of the 50 MHz. clock that the state machine waits before transitioning. The count when '0' selects continuous mode. When programmed to a non-zero value a specific number of pulses are generated.

If desired, the interrupt can be enabled and the interrupt vector written to the vector register. The interrupt vector is not used in many systems and is provided to support the IP specification and older systems requiring the vector.

A typical sequence using a vector would be to first write to the vector register with the desired interrupt vector. For example, $40 is a valid user vector for the Motorola 680x0 family. The interrupt service routine should be loaded and the mask should be set. The hardware will hold the interrupt status until explicitly cleared with software.

Important programming note: The Master enable and local enables are re-synchronized to the reference oscillator in hardware. Those bits can be set/cleared at any time. New in revision D, the time off, time on, shift and pulse count bits registers are synchronized to the pulse generation state-machine. Parameters can be updated at any time. The new control definitions require the appropriate bit(s) in the Pulse Control Register to be set to take effect.

For synchronous changes, the parameters should be updated for the channels to be affected then the enable bits set. The new parameters will be implemented the next time the parameters are used. For example if the shift enable is set, the time will be added to the OFF time. If the pulse is currently in the on state, nothing will happen until the next off time. If the interrupt on every pulse capability is enabled; the software can tell where the end of a pulse is, and can assert the parameter enable such that several channels are updated in synchronization with each other. If the master interrupt enable is disabled polling can be used. If the channels are being used independently the parameters can be updated at any time.

Register Definitions

IP_PARPLS_BASE

$00 Pulse Control Register Port read/write

Base Control Register

DATA BIT	DESCRIPTION
15-8	spare
7	Interrupt Enable Channel 3
6	Interrupt Enable Channel 2
5	Interrupt Enable Channel 1
4	Interrupt Enable Channel 0
3	spare
2	Interrupt request Force
1	Master Interrupt Enable
0	Master Pulse Generator Enable

FIGURE 2 IP-PULSE BASE CONTROL REGISTER 0 BIT MAP

0 . When Master_Enable = '1' the pulse generators channels(4) are enabled to operate based on the local enable and the channels control registers. To synchronize the channels – set and enable the local channels then enable the Master_Enable. Clearing the Master_Enable will abort all channels in the next "off" phase.

1. Master Interrupt Enable when '1' allows the local interrupt enables to reach the IP interrupt request. Leave disabled to use the status register for polled operation.

2. Force Interrupt when '1' and Master Interrupt is enabled causes an interrupt request independent of any channel activity. Useful for software debugging and hardware test. Clear to remove the interrupt request. Leave '0' for normal operation.

7-4. Individual Channel Interrupt enables. When '1' and Master is enabled the interrupt for the associated channel causes an interrupt to the host. Read the status register for the cause of the interrupt. Clear by writing to the status register.

IP_PARPLS_STAT

$02 Pulse Status Register Port read/write

Status Register	
DATA BIT	DESCRIPTION
15-4	undefined
3	IntCh3
2	IntCh2
1	IntCh1
0	IntCh0

FIGURE 3 IP-PULSE STATUS REGISTER BIT MAP

IntChX When set an interrupt is pending for channel X. Clear by writing a '1' back to the same bit position(s). The interrupt indicates that the programmed operation for that channel is completed or [if enabled] an additional period of the pulse defined for that channel has completed.

IP_PARPLS_TOFFx_L

$10,20,30,40 Pulse Time Off Lower Register Port read/write

Time Off Lower Registers	
DATA BIT	DESCRIPTION
15-0	lower 16 Time Off Bits

FIGURE 4 IP-PULSE TIME OFF LOWER BIT MAP

IP_PARPLS_TOFFx_U

$12, 22, 32, 42 Pulse Time Off Upper Register Port read/write

Time Off Upper Registers	
DATA BIT	DESCRIPTION
15-12	Spare
11-0	Upper 12 Time Off Bits

FIGURE 5 IP-PULSE TIME OFF UPPER BIT MAP

The Upper and Lower Time Off registers are concatenated to create a 28 bit [27-0] Time-Off definition. Time Off is literally the time when the pulse is not enabled. The time is set with the following formula Time = (N+2)* 20 nS. Or
N = (Time desired/20 nS) – 2. In some cases you will have to approximate the value to the nearest 20 nS period.

Please note that the "OFF" time does not take effect until the "OFF Enable" is set in the PCCR.

IP_PARPLS_TONx_L

$14,24,34,44 Pulse Time On Lower Register Port read/write

Time On Lower Registers	
DATA BIT	DESCRIPTION
15-0	lower 16 Time On Bits

FIGURE 6 IP-PULSE TIME ON LOWER BIT MAP

IP_PARPLS_TONx_U

$16,26,36,46 Pulse Time On Upper Register Port read/write

Time On Upper Registers	
DATA BIT	DESCRIPTION
15-12	Spare
11-0	Upper 12 Time On Bits

FIGURE 7 IP-PULSE TIME ON UPPER BIT MAP

The Upper and Lower Time On registers are concatenated to create a 28 bit [27-0] Time-On definition. Time On is literally the time when the pulse is enabled. The time is set with the following formula Time = (N+2)* 20 nS. Or
N = (Time desired/20 nS) – 2. In some cases you will have to approximate the value to the nearest 20 nS period.

With a value of 0 for N, an approximately 40 nS wide pulse is generated. With TOFF also programmed to 0 a square wave of 80 nS is generated with 40 on and 40 off.

Please note that the “ON” time does not take effect until the “On Enable” is set in the PCCR.

Please note that the buffers are not exactly symmetrical leading to slightly different periods than programmed. The symmetry induced error is a constant and improves as the programmed period increases. The times are exact at the FPGA pin.

IP_PARPLS_PCCRx_L

$18,28,38,48 Pulse Count Control Lower Register Port read/write

Time Off Lower Registers	
DATA BIT	DESCRIPTION
15-0	lower 16 Count

FIGURE 8 IP-PULSE PCCR LOWER BIT MAP

IP_PARPLS_PCCRx_U

$1A, 2A, 3A, 4A Pulse Count Control Upper Register Port read/write

Time Off Upper Registers	
DATA BIT	DESCRIPTION
15	local Enable
14	Interrupt On each pulse generated
13	Invert Waveform
12	spare
11	spare
10	On Time Enable
9	Off Time Enable
8	Shift Enable
7-0	Upper 8 Count

FIGURE 9 IP-PULSE PCCR UPPER BIT MAP

The Upper and Lower PCCR registers are concatenated to create a 24 bit [23-0] Count definition plus channel specific control bits.

(31)15. Local Enable when '1' allows the associated channel to begin transmitting if the Master Enable is set to '1'. For independent operation leave the master enable set to '1'. The local enables will then start each channel when set. For synchronized operation clear the Master Enable '0' until the channels are set-up and enabled then use the Master Enable to start operation.

The local Enable is auto-cleared at the end of the programmed operation. Software can clear the bit to abort a particular channel. The channel complete interrupt will occur when the channel stops operation.

(30)14. When set the channel will create an interrupt request for each pulse that is generated. Be careful if you have a short period for your pulse generation. You may miss interrupts if your software can't process faster than the interrupts are generated.

(29)13. When set the pulse will be active low instead of active high. Time Off corresponds to time low. Time On corresponds to Time high. The inversion takes place after the pulse is generated internally to effectively reverse the On/Off relationship.

(26)10. When set the State Machine will reload the reference value for the "On Time". The bit should be set after both of the associated registers have been updated. The bit is auto-cleared after the value has been captured for state-machine use. Updating the value more often than the state-machine uses the value will result in lost updates.

(25)9. When set the State Machine will reload the reference value for the "OFF Time". The bit should be set after both of the associated registers have been updated. The bit is auto-cleared after the value has been captured for state-machine use. Updating the value more often than the state-machine uses the value will result in lost updates.

(24)8. When set the State Machine will implement the shift count value. The bit should be set after the associated register has been updated [if the value is to be changed]. The bit is auto-cleared after the value has been captured for state-machine use. Updating the value more often than the state-machine uses the value will result in lost requests.

7-0 plus 15-0 create the count definition 23-0. Each count represents one "Off" followed by one "On" period. Programming the count to "0" will put the state machine into infinite mode where there is no end count. In this mode the software will need to stop transmission by aborting the master or local enables.

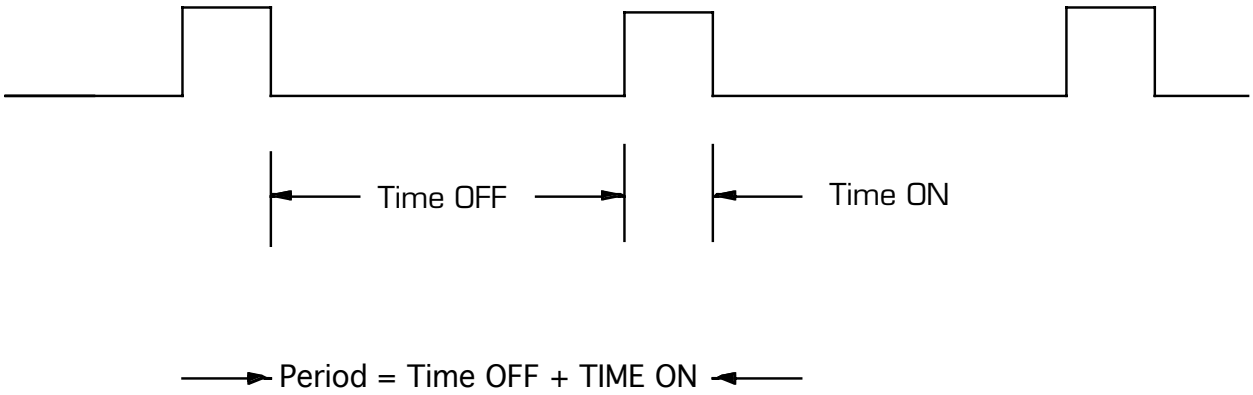


FIGURE 10 IP-PULSE TIMING DEFINITION

IP_PARPLS_shft

$1C, 2C, 3C, 4C Shift Time write only

Time On Lower Registers	
DATA BIT	**DESCRIPTION**
15-0	16 Shift Time Bits

FIGURE 11 IP-PULSE SHIFT TIME BIT MAP

The Shift time registers are 16 bits wide. The Shift time is the amount of time to add to the off time each time the Shift Enable is set in the PCCR. The time is set with the following formula Time = (N+2)* 20 nS. Or
N = (Time desired/20 nS) – 2. In some cases you will have to approximate the value to the nearest 20 nS period.

IP_PARPLS_VECT

$06 Parallel Interrupt Vector Port

The Interrupt vector for the IP-Pulse is stored in this byte wide register. This read/write register is initialized to 'xxFF' upon power-on reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered.

Interrupts

All IP Module interrupts are vectored. The vector from the IP-PULSE comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-PULSE state machines generate an interrupt request when a programmed condition is detected. The interrupt is mapped to interrupt request 0. The CPU can respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector when accessed by the CPU. The source of the interrupt is obtained by reading IP_PARPLS_STAT. The status remains valid explicitly cleared. There is an interrupt defined for each channel. The status register should be read first to determine which interrupt types are active. The exception handler can then respond to all of the current interrupt requests.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the IP_PARPLS_BASE register. The individual enables are controllable through PCCRx. Once the interrupt request is set, the way to clear the request is to write to the status register with the bit corresponding to the interrupt set. The Interrupt acknowledge cycle fetches the vector, but does not clear the interrupt request in this design.

For Auto-vectored operation; read the status register in response to an interrupt request. Clear the interrupt(s) by writing the same bits back to the status register.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled. The status is latched until cleared by the software.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision to be present, it may check for it directly. The software interface for each of the versions of the IP-Pulse are identical. One ID PROM version is used in all cases.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-PULSE is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-Pulse board will be recorded with a new code in the DRIVER ID and reserved fields.

Address	Definition	Value
01	ASCII "I"	$49
03	ASCII "P"	$50
05	ASCII "A"	$41
07	ASCII "H"	$48
09	Manufacturer ID	$1E
0B	Model Number	$03
0D	Revision	$B0
0F	reserved	$00
11	Driver ID, low byte	$00
13	Driver ID, high byte	$10
15	No of extra bytes used	$0C
17	CRC	$8F

FIGURE 12 IP-PULSE ID PROM

IP-Pulse Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-PULSE. Pins marked n/c below are defined by the specification, but not used on the IP-PULSE. Also see the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		DMAReq0*		5		30	
	D2		MEMSEL*		6		31
D3		DMAReq1*		7		32	
	D4		IntSel*		8		33
D5		DMAck*		9		34	
	D6		IOSel*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		DMAEnd*		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		IntReq0*		17		42	
	D14		A4		18		43
D15		IntReq1*		19		44	
	BS0*		A5		20		45
BS1*		n/c		21		46	
	n/c		A6		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		GND		25		50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 13 IP-PULSE LOGIC INTERFACE

IP-Pulse IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PULSE. Pins marked. Also see the User Manual for your carrier board for more information.

CH0+		1		26	
	CH0-		2		27
		3		28	
			4		29
CH1+		5		30	
	CH1-		6		31
		7		32	
			8		33
CH2+		9		34	
	CH2-		10		35
		11		36	
			12		37
CH3+		13		38	
	CH3-		14		39
		15		40	
			16		41
		17		42	
			18		43
		19		44	
			20		45
		21		46	
			22		47
		23		48	
			24		49
GND	GND	25		50	

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 14 IP-PULSE IO INTERFACE

Please note that the + side corresponds to the TTL output for –TTL, -1, -2, -3 versions.

Type	Channel Population
–TTL	CH0, CH1, CH2, CH3 = TTL/CMOS outputs
–1	CH0 = 422, CH1-3 = TTL/CMOS
–2	CH0, CH1 = 422, CH2, CH3 = TTL/CMOS
–3	CH0-2 = 422, CH3 = TTL/CMOS
–422	CH0, CH1, CH2, CH3 = 422 outputs

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. Other than series resistors for the "TTL" interface the IP-Pulse does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Integrated circuits can be damaged by static discharge. Proper anti-static handling proceedures must be followed.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

IndustryPacks® are mezzanine cards which require an adapter to work in any system. IP Modules are commonly used and frequently systems have "extra" slots where the modules can be located. Dynamic Engineering manufactures carriers for the PCI, PC/104p and cPCI buses. Please check our website for new carriers not released at the time this manual was published.

IndustryPacks are portable and can be used on third party carriers when the hardware is compliant with the IP specification.

http://www.dyneng.com/pci_3_ip.html
http://www.dyneng.com/pci5ip.html
http://www.dyneng.com/cpci2ip.html
http://www.dyneng.com/cpci4ip.html
http://www.dyneng.com/pc104p4ip.html

Different platforms have different operating system requirements. If you need a driver please contact Dynamic Engineering. Dynamic Engineering has driver expertise for Windows NT, 2000, and XP. Dynamic Engineering also writes drivers for Linux and has plans for VxWorks and Labview. We can support your effort with driver and application software or help for your software designers. Dynamic Engineering hardware designs have features to help the integrator to write and test their software quickly and efficiently – we can help you.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-PULSE is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required. Dynamic Engineering IndustryPack Modules are shipped with a mounting kit.. [IP-MTG-KIT is available if you misplace the mounting hardware or if another IP was not shipped with the standoffs and screws]

The IP Module provides a low temperature coefficient of 0.89 W/^{0}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{0}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-Pulse design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering

435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
e-mail support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Features:	Up to 4 pulse generators with either TTL or Differential IO. 64 mA sink with 10 mA pull-up. 20 nS resolution. 28 bit time off and time on registers. 16 bit phase shift register. Continuous output or programmed [24 bit count]. Independent channels.
Software Interface:	Control Registers, ID PROM, Vector Register, Status Port
Initialization:	Hardware Reset initializes all registers.
Access Modes:	Word I/O Space (see memory map) Word in ID Space auto-vectored interrupt
Access Time:	back-to-back cycles in 500ns (8Mhz.) or 125 nS (32 Mhz.)
Wait States:	1 to all spaces
Interrupt:	interrupt on completion of programmed pulse count interrupt on pulse generated separate interrupt and status per channel
DMA:	No Logic Interface DMA Support implemented at this time.
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface [HDRterm50] User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{0}C for uniform heat across IP
Power:	Typical **52** mA @ 5V unloaded. Additional current will be required depending on the loads applied

Order Information

The IP-Pulse board has 5 standard configurations.
http://www.dyneng.com/ip_pulse.html

"**-TTL**"	4 TTL pulse generators [open drain with 470Ω to 5V]
"**-1**"	3 TTL and 1 422 pulse generators
"**-2**"	2 TTL and 2 – 422 pulse generators
"**-3**"	1 TTL and 3 – 422 pulse generators
"**-422**"	4 – 422 pulse generators

Tools for IP-PULSE

IP-Debug-Bus - IP Bus interface extender with testpoints, isolated power & quickswitch technology to allow hot swapping or power cycling without powering down the host. http://www.dyneng.com/ipdbgbus.html

IP-Debug-IO II - IndustryPack IO connector breakout with testpoints, ribbon cable headers, and locations for user circuits. http://www.dyneng.com/ipdbgio.html

HDRterm50 - Ribbon cable compatible 50 pin header to 50 screw terminal header. Comes with DIN rail mounting capability. http://www.dyneng.com/HDRterm50.html

HDRribn50 – Ribbon cable in several standard lengths plus custom, with strain relief and cable pull attached. http://www.dyneng.com/HDRribn50.html

PCI3IP - 1/2 length PCI card with 3 IP slots. http://www.dyneng.com/pci_3_ip.html

PCI5IP - PCI card with 5 IP slots. http://www.dyneng.com/pci5ip.html

cPCI2IP - cPCI card with 2 IP slots. http://www.dyneng.com/cpci2ip.html

cPCI4IP - cPCI card with 4 IP slots. http://www.dyneng.com/cpci4ip.html

IP-MTG-KIT – 4 metric stainless screw and stand-off pairs to retain IP-Pulse against the carrier board. Flat head screws match IP Specification mounting requirements.
http://www.dyneng.com/IPHardware.html

Off the shelf ribbon cables and custom cables are available.