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User Manual

IP-Parallel-HV-Miller

Miller-Encoded Serial Data Interface
IP Module

Revision A
Corresponding Hardware: Revision B
10-2001-0302

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Miller-Encoded Serial Data Interface
IP Module

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This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

IP-Parallel-HV is part of the IP Module family of modular I/O components. The IP-Parallel-HV is capable of providing multiple protocols. The standard version provides 24 uncommitted outputs and 24 uncommitted inputs. The outputs utilize LSO7's to provide a high voltage low side switch. The on-board regulator provides a 6.5V standard reference. Other voltages can be supplied up to 12V. An external supply can be used when desired or if voltages above 12V need to be generated. Each input channel has a resistor divider to scale the input voltage back to "TTL" levels. The resistors can be altered for other voltage requirements.

The IP-Parallel-HV-Mlr has been modified to provide one input and one output channel with single-ended TTL I/O voltage levels. The single ended driver signal is characterized as an open drain driver with 24 mA of sink. A 470Ω pull-up to +5v is supplied on-board.

The IP-Parallel-HV-Mlr supports both 8 and 32 MHz IP Bus operation. The on-board oscillator is used to derive the reference clocks for the Tx and Rx serial operation. All configuration registers support read and write operations for maximum software convenience. Word and byte operations are supported (please refer to the memory map).

The IP-Parallel-HV-Mlr conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. The PCI3IP card makes a convenient development platform in many cases.
http://www.dyneng.com/pci_3_ip.html

Various transmit and receive interrupts are supported by the IP-Parallel-HV-Mlr. There are interrupts for transmission complete, data received, transmit FIFO almost empty, receive FIFO almost full, receive FIFO overflow, and loss of receive signal. All the interrupts can be individually enabled by separate control bits in the configuration registers. The interrupt vector is user programmable by a read/write register. The interrupt occurs on IntReqO and the vector can be read in the IO space or automatically with the INT space select strobe. The interrupt status bits are available in the

interrupt status register even if the interrupt enable bits are not set. This allows the host to operate by polling rather than causing a system interrupt.

The serial transmit channel reads data from the output FIFO and sends it out serially, msb first. Data can be pre-stored in the FIFO and sent later with the Tx start bit. When the receiver is enabled it will look for the PCM header (0xBA00) to determine when a data-word is written to the FIFO.

Theory of Operation

The IP-Parallel-HV-Mlr is designed for the purpose of transferring data from one point to another with a Miller encoded serial protocol.

The IP-Parallel-HV-Mlr features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the IP-Parallel-HV-Mlr design. Only the voltage regulators, drivers, receiver and boot PROM are external to the Xilinx device.

The IP-Parallel-HV-Mlr is part of the IP Module family of modular I/O products. It meets the IP Module Vita Standard. In standard configuration it is a Type 1 mechanical with no components on the back of the board and one slot wide. Contact VITA for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and basic logic design.

A logic block within the Xilinx device contains the decoding and timing elements required for the host CPU to interface with the IP bus. The timing is referenced to the 8 or 32 MHz IP logic clock. The IP responds to the ID, INT, MEM, and IO selects. The DMA control lines are connected to the Xilinx for future revisions, but are not used at this time. The Parallel-HV-Mlr design requires two wait states for read or write cycles to any address. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host removes the SEL line. Local timing terminates a write cycle prior to the SEL being deasserted. If no hold cycles are requested by the host, the IP-Parallel-HV-Mlr is capable of supporting 16+ MB per second data transfer rate with a 32 MHz reference rate.

The parallel I/O can support many protocols. The Miller timing is shown in figure 1. Miller-code data is determined solely by the interval between signal transitions. The only valid intervals are one, one and one-half, and two bit-periods. An interval of one bit-period indicates that the current data-bit is the same as the previous one. An interval of one and one-half bit-periods indicates a '1' if the previous data was a '0' or a "OO" sequence if the previous data was a '1'. An interval of two bit-periods will be seen when a "O1" sequence follows a previous '1'.

The transmit state machine uses a programmed reference clock running at 2x the transmit data rate to create the required signal intervals. When the transmit state machine is started, data is read out of the FIFO and encoded into the Miller protocol and sent out on the Tx Data lines, msb first. If the HOWINST interface (32-bit) is selected, the data is used directly from the FIFO. If the HDAM interface (34-bit) is selected, a "10" is prepended to the FIFO word to create the upper two bits of the 0xBA00 PCM header. The remaining 32 bits are taken directly from the FIFO to form the 34-bit data word. This process continues until there is no more data in the FIFO at which point the Tx interrupt occurs, if enabled, and the transmit state machine transmits zeros until it is disabled. If messages longer than the Tx FIFO size are desired, the Tx almost empty interrupt can be used to signal the loading of additional data before the FIFO becomes empty.

The IP-Parallel-HV-Mlr receiver uses a 32x clock to detect signal transition intervals in the received data stream. An interval of up to 40 32x clocks is interpreted as a one-clock interval. An interval of 41-56 32x clocks is interpreted as a one and one-half clock interval. An interval of 57-80 clocks is interpreted as a two-clock interval. And an interval of 81 or more clocks is interpreted as a no-data condition and will cause the receiver loss-of-signal status to be set. The receiver monitors the input data stream looking for the PCM header value of 0xBA00. When this value is seen a 32-bit value is written to the receive FIFO. If the HOWINST interface (32-bit) is selected, the entire data-word is written to the FIFO. If the HDAM interface (34-bit) is selected, only the lower 32-bits of the data-word are written to the FIFO ("11101000000000" + 18 bits of data).
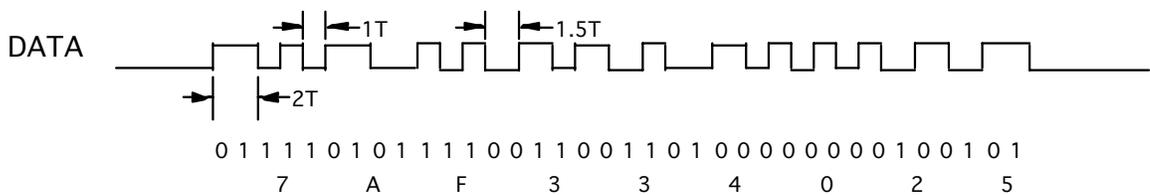
FIGURE 1   IP-PARALLEL-HV-MLR SERIAL PROTOCOL TIMING

When the receiver detects a valid data-word, an Rx interrupt will occur, if enabled. This signals the user that at least one data-word is available to be read from the Rx FIFO. Messages larger than the FIFO size can be handled using the Rx almost full interrupt to read the data from the Rx FIFO before it becomes full and causes a data overrun error condition to occur.

The FIFO level status is also available from the FIFO status register if it is desired to run in a polled mode without interrupts. The data counts from the transmit and receive FIFO are available as well.

Some IP Carriers support 32-bit data writes to IP slots performing an auto-conversion to 16 bits saving half of the bus accesses. The PCI3IP and PCI5IP support auto-incrementing and static address conversion from 32 to 16 bits.

Address Map

Function	Offset	Width	Type
IPPHV_MLR_BASE	0x00	word	read/write
IPPHV_MLR_TX_CONTROL	0x02	word	read/write
IPPHV_MLR_RX_CONTROL	0x04	word	read/write
IPPHV_MLR_VECTOR	0x06	byte	read/write
IPPHV_MLR_STATUS	0x08	word	read
IPPHV_MLR_INTSTAT	0x0A	word	read/write
IPPHV_MLR_RX_AFL_COUNT	0x0C	word	read
IPPHV_MLR_TX_AMT_COUNT	0x0E	word	read
IPPHV_MLR_FIFO_PORT	0x10	word	read/write
IPPHV_MLR_RX_DATA_COUNT	0x12	word	read
IPPHV_MLR_TX_DATA_COUNT	0x14	word	read

FIGURE 2   IP-PARALLEL-HV-MLR INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-Parallel-HV-Mlr. The addresses are all offsets from the IO space base address. The TX and RX FIFO ports are also mapped to the entire MEM address space and the IP-Parallel-HV-Mlr IDPROM is mapped to the ID space. The carrier board that the IP is installed into provides these addresses.

Programming

Programming the IP-Parallel-HV-Mlr requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Carrier board. In this document, the base address refers to the starting address of the IO space of the slot in which the IP is installed. The receive and transmit FIFOs are mapped to the entire MEM space to allow data blocks to be read and written without regards to address incrementing issues.

In order to receive data the software is only required to enable the receiver. If interrupts are desired, the master interrupt and individual interrupts of interest can be enabled and the interrupt vector written to the vector register. Data will be loaded into the receive FIFO as it is received.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example $40 is a valid user vector for the Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the interrupt mask set. When the receiver start bit is set, the hardware looks for a PCM header match. Once the header is detected the data is loaded into the FIFO and an interrupt request can be asserted to let the host know that data is available. The software can set up a loop counter to efficiently read the data from the FIFOs. If continuous data is expected the PAF interrupt may be more interesting. Using the PAF interrupt would allow larger data blocks to be moved from the IP-Parallel-HV-Mlr to host memory.

REGISTER DEFINITIONS

IPPHV_MLR_BASE

0x00 Base Control Register Port - read/write

Base Control Register	
Data Bit	Description
15-4	Spare
3	FIFO Reset
2	FIFO Bypass Enable
1	Force Interrupt
0	Master Interrupt Enable

FIGURE 3   IP-PARALLEL-HV-MLR BASE CONTROL REGISTER BIT MAP

Master Interrupt Enable: Defaults to '0' (disabled). If this bit is set to '1' (enabled) then the Rx and Tx interrupts can occur based on individual interrupt enables. If this bit is set to '0', then no interrupts will be generated. The status register will still report the individual interrupt conditions to allow polled operation.

Force Interrupt: Defaults to '0' (disabled). This bit is used to create an interrupt for test and software development purposes. Set the bit to cause the interrupt and clear the bit to remove the interrupt. Requires the master interrupt enable to be '1' to have an effect.

FIFO Bypass Enable: Defaults to '0' (disabled). If this bit is set to '1' (enabled) then data written to the Tx FIFO is automatically transferred to the Rx FIFO. This allows the Tx and Rx FIFOs to be tested by writing to the Tx FIFO and Reading from the Rx FIFO. The IP MEM space is mapped to the FIFO ports, which allows block transfers to be accomplished easily.

FIFO Reset: Defaults to '0' (disabled). Set this bit to a '1' to reset the Tx and Rx FIFOs and associated circuitry. Set this bit to a '0' for normal operation.

IPPHV_MLR_TX_CONTROL

0x02 Tx Control Register Port - read/write

Tx Control Register	
Data Bit	**Description**
15-4	Spare
2	Tx FIFO Almost Empty Interrupt Enable
1	Tx Interrupt Enable
3	Tx Interface Select
0	Tx Start

FIGURE 4   IP-PARALLEL-HV-MLR TX CONTROL REGISTER BIT MAP

Tx Start: Defaults to '0' (disabled). When this bit is set to '1' (enabled),
The transmitter begins to send data. If no data is present in the Tx FIFO,
zeros will be sent until valid data is written to the FIFO or the transmitter is
disabled. When data is present in the FIFO and the transmitter is enabled,
The data will be read from the FIFO and transmitted serially MSB first.
When the FIFO becomes empty, zeros will continue to be transmitted and a
Tx done pulse will occur, which can be configured to cause an interrupt.

Tx Interface Select: Defaults to '0' (32-bit Interface). This bit is used to
select the length of the Transmitted word. When this bit is set to '0', the
transmitter reads two 16-bit words from the Tx FIFO and sends 32 bits of
data out serially, MSB first. When this bit is set to '1', the transmitter
reads two 16-bit words from the Tx FIFO as before, but then a "10" is
appended to the top of the word to form a 34-bit word that is then sent
out serially, MSB first. Since 0xBA00 is used as a header to indicate the
beginning of a data word, writing 0xE8000000 to the FIFO will result in the
header value followed by 18 zeros. Note: The most significant 16-bit word
is written first and read first from the FIFO.

Tx Interrupt Enable: Defaults to '0' (disabled). When this bit is set to '1'
(enabled), the transmitter can generate an interrupt when the FIFO data is
exhausted. In order for an interrupt to occur, the master interrupt enable
must also be enabled. When this bit is set to '0', the transmit interrupt
will not be asserted, but the appropriate status bit in the interrupt status
register will still be latched when the transmission is complete.

Tx FIFO Almost Empty Interrupt Enable: Defaults to 'O' (disabled). When this bit is set to '1' (enabled), an interrupt can be generated when the Tx FIFO goes below the almost empty level set in the IPPHV_MLR_TX_AMT_COUNT register. In order for an interrupt to occur, the master interrupt enable must also be enabled. When this bit is set to 'O', the almost empty interrupt will not be asserted, but the appropriate status bit in the interrupt status register will still be latched when the Tx FIFO goes below the almost empty level.

IPPHV_MLR_RX_CONTROL

0x04 Rx Control Register Port - read/write

Rx Control Register	
Data Bit	Description
15-6	Spare
5	Rx Loss-of-Signal Interrupt Enable
4	Rx FIFO Overflow Interrupt Enable
3	Rx FIFO Almost Full Interrupt Enable
2	Rx Interrupt Enable
1	Rx Interface Select
0	Rx Start

FIGURE 5   IP-PARALLEL-HV-MLR RX CONTROL REGISTER BIT MAP

Rx Start: Defaults to 'O' (disabled). When this bit is set to '1' (enabled), The receiver will begin to look for data. When the PCM header (OxBAOO) is detected, 32-bits of data will be written to the Rx FIFO. If the 32-bit interface is selected, the entire data word will be written. If the 34-bit interface is selected the most significant two bits ("1O") will be stripped off and the remaining 32-bits of data will be written. When this bit is set to 'O' the receiver will stop monitoring the data stream.

Rx Interface Select: Defaults to 'O' (32-bit Interface). This bit is used to select the length of the Received data word. When this bit is set to 'O' and the header data is received, the header and the following 16 data bits will be written to the Rx FIFO. When this bit is set to '1' (34-bits) and the header is received, the lower 14 bits of the header and the following 18

data bits will be written to the Rx FIFO.

Rx Interrupt Enable: Defaults to 'O' (disabled). When this bit is set to '1' (enabled), the receiver can generate an interrupt when a data value is written to the Rx FIFO. In order for an interrupt to occur, the master interrupt enable must also be enabled. When this bit is set to 'O', the receive interrupt will not be asserted, but the appropriate status bit in the interrupt status register will still be latched when a data word is received.

Rx FIFO Almost Full Interrupt Enable: Defaults to 'O' (disabled). When this bit is set to '1' (enabled), an interrupt can be generated when the Rx FIFO goes above the almost full level set in the IPPHV_MLR_RX_AFL_COUNT register. In order for an interrupt to occur, the master interrupt enable must also be enabled. When this bit is set to 'O', the almost full interrupt will not be asserted, but the appropriate status bit in the interrupt status register will still be latched when the Rx FIFO becomes almost full.

Rx FIFO Overflow Interrupt Enable: Defaults to 'O' (disabled). When this bit is set to '1' (enabled), an interrupt can be generated when an attempt is made to write to the Rx FIFO when it is full. In order for an interrupt to occur, the master interrupt enable must also be enabled. When this bit is set to 'O', the overflow interrupt will not be asserted, but the appropriate status bit in the interrupt status register will still be latched when the Rx FIFO overflows.

Rx Loss-of-Signal Interrupt Enable: Defaults to 'O' (disabled). When this bit is set to '1' (enabled), an interrupt can be generated when a transition in the data stream is not seen for 10 microseconds (the maximum interval in the data stream is 8.13 microseconds). In order for an interrupt to occur, the master interrupt enable must also be enabled. When this bit is set to 'O', the loss-of-signal interrupt will not be asserted, but the appropriate status bit in the interrupt status register will still be latched when the Rx signal stops.

IPPHV_MLR_VECTOR

0x06 Interrupt Vector Port read/write

The interrupt vector for the IP Parallel-HV-Mlr is stored in this byte wide register. This read/write register is initialized to 0XFF upon power-on reset or software reset. The vector is stored in the odd byte location (D7..0) and should be initialized before the interrupt is enabled or the mask is lowered.

IPPHV_MLR_STATUS

0x08 FIFO Status Port - read only

Status Register	
Data Bit	**Description**
15-11	Spare
10	Aux Data 2
9	Aux Data 1
8	Aux Data 0
7	Tx FIFO Full
6	Tx FIFO Almost Empty
5	Tx FIFO Data Valid
4	Tx FIFO Empty
3	Rx FIFO Full
2	Rx FIFO Almost Full
1	Rx FIFO Data Valid
0	Rx FIFO Empty

FIGURE 6   IP-PARALLEL-HV-MLR FIFO STATUS REGISTER BIT MAP

Rx FIFO Empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Rx FIFO Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO is empty, because as soon as a word is written into the FIFO, it is read out to be ready for an IP read cycle. When this bit is a zero, it indicates that there is no receive data available.

Rx FIFO Almost Full: When a one is read, the number of data words in the

receive data FIFO is greater or equal to the value written to the IPPHV_MLR_RX_AFL_COUNT register; when a zero is read, the level is less than that value.

Rx FIFO Full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Tx FIFO Empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Tx FIFO Data Valid: When a one is read, there is at least one valid transmit data word left. This bit can be set even if the Tx FIFO is empty, because as soon as two 16-bit words are written into the FIFO, a 32-bit word is read out to be ready for the Tx state machine. When this bit is a zero, it indicates that there is no transmit data remaining.

Tx FIFO Almost Empty: When a one is read, the number of data words in the transmit data is less than or equal to the value written to the FIFO IPPHV_MLR_TX_AMT_COUNT register; when a zero is read, the level is more than that value.

Tx FIFO Full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Aux Data O-2: These three bits can be used for general purpose TTL inputs. They are driven from I/O pins 39-41 (see Figure 10 page 26).

IPPHV_MLR_INTSTAT

0xOA Interrupt/Error Status Port - read/write

Status Register	
Data Bit	Description
15	Interrupt Active
14	Interrupt Status
13-6	Spare
5	Rx Loss-of-Signal Interrupt
4	Rx FIFO Overflow Interrupt
3	Rx FIFO Almost Full Interrupt
2	Tx FIFO Almost Empty Interrupt
1	Rx Interrupt
0	Tx Interrupt

FIGURE 7   IP-PARALLEL-HV-MLR INTERRUPT STATUS REGISTER BIT MAP

All of the bits in this register have corresponding enables in the Tx/Rx control registers that can be set to cause an interrupt when the condition occurs, but the status value can be read regardless of the interrupt enable state. All individual interrupt status bits are latched when the respective interrupt condition occurs. In order to clear these latched bits, write the appropriate bit value back to this register address.

Tx Interrupt: When this bit is read as a one, a transmission has begun and completed since the bit was last cleared. When the bit is read as a zero, either the transmission was not started or it has not yet completed since the bit was last cleared.

Rx Interrupt: When this bit is read as a one, at least one data-word has been received since the bit was last cleared. When the bit is read as a zero, no valid data has been received since the bit was last cleared.

Tx FIFO Almost Empty Interrupt: When this bit is read as a one, the transmit FIFO data count has transitioned from greater than to less than or equal to the level set in the PMC_SPWR_TX_AMT register. When the bit is read as a zero, the level has not crossed this threshold since the bit was last cleared.

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Rx FIFO Almost Full Interrupt: When this bit is read as a one, the receive FIFO data count has transitioned from less than to greater than or equal to the level set in the PMC_SPWR_RX_AFL register. When the bit is read as a zero, the level has not crossed this threshold since the bit was last cleared.

Rx FIFO Overflow Interrupt: When this bit is read as a one, an attempt was made to write to the receive FIFO when the FIFO was already full. When the bit is read as a zero, the receive FIFO has not experienced a data overrun since the bit was last cleared.

Rx Loss-of-Signal Interrupt: When this bit is read as a one, an interval in the receive data stream greater than 10 microseconds was seen. When the bit is read as a zero, there were no intervals greater than 10 microseconds since the bit was last cleared. The largest interval seen in the normal data stream is 8.13 microseconds, so an interval of 10 microseconds is interpreted as a loss-of-signal event.

Interrupt Status: When this bit is read as a one, it indicates that an enabled interrupt condition has occurred. If the master interrupt enable is enabled, then the interrupt request will be driven onto the IP bus, if not no interrupt will occur. This bit is not latched.

Interrupt Active: When this bit is read as a one, it indicates that the interrupt for this card is being asserted onto the IP bus. This bit is also not latched.

IPPHV_MLR_RX_AFL_COUNT

0x0C Rx FIFO Almost Full Count Register Port – read/write

When the number of data-words in the Rx FIFO is greater or equal to the data value stored in this register, the Receive FIFO almost full status will be true.

IPPHV_MLR_TX_AMT_COUNT

0x0E Tx FIFO Almost Empty Count Register Port – read/write

When the number of data-words in the Tx FIFO is equal to or less than the data value stored in this register, the Transmit FIFO almost empty status will be true.

IPPHV_MLR_FIFO_PORT

0x10 FIFO Data Port - read/write

Data to be written to the Transmit FIFO is written to this port. A write to the Memory space (any address) will also access this port.

The data stored in the Receive FIFO can be accessed through this port. A read from the Memory space (any address) will also access this port.

Use the memory space for 32-bit auto-incrementing accesses and faster transfers if your carrier supports that. Non-compelled DMA is also an option with the MEM space access.

IPPHV_MLR_RX_DATA_COUNT

0x12 Rx FIFO Data Count Port – read only

The value read from this status register represents the number of 16-bit words that are present in the receive FIFO.

IPPHV_MLR_TX_DATA_COUNT

0x14 Tx FIFO Data Count Port – read only

The value read from this status register represents the number of 16-bit words that are present in the transmit FIFO.

INTERRUPTS

All IP Module interrupts are vectored. The vector from the IP-Parallel-HV-Mlr comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8-bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-Parallel-HV-Mlr state-machines generate an interrupt request when a transmission is complete or data is received and the appropriate enable bit in the control registers are set. The transmission is considered complete when the last bit is clocked out. The interrupt is mapped to interrupt request O. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector. The source of the interrupt is obtained by reading the Interrupt status register. The status remains valid until the status register bits are cleared. The interrupt remains asserted until the status is cleared, or the interrupt enables are disabled.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the base control register. The individual enables for Tx and Rx are controllable through their respective control registers. The enables operate after the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to clear the interrupt status latch or disable the interrupt. The bits must be cleared or the particular interrupt disabled before the Master interrupt enable is re-asserted or another interrupt will be generated. The interrupt enables can be set back to enabled immediately after clearing the status bits. Tx Interrupt Enable enables the Tx interrupt and Rx Interrupt Enable enables the Rx interrupt.

If operating in a polled mode and making use of the interrupts for status then the interrupts should be disabled and the interrupt status register polled. When the interrupt status shows an interrupt pending the appropriate FIFO action can take place, then the appropriate status bit is written back to clear that "interrupt request" before starting the next transfer.

Power on initialization will provide a cleared interrupt request, interrupts disabled, and interrupt vector of $FF.

The programmable FIFO interrupts operate in much the same way. The programmable interrupts are triggered by FIFO levels instead of Tx / Rx events. The interrupts are cleared by writing to the interrupt status register. The levels are programmable to allow the software to respond before the FIFO is empty or full so that longer transfers can be handled without using larger FIFOs.

Loop-back

The Engineering kit has reference software, which includes external loop-back tests. The tests require an external cable with the following pins connected.

Tx->Rx Data   13 - 38

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID
PROM aids in software auto configuration and configuration management.
The user's software, or a supplied driver, may verify that a particular device
is actually installed at the location it expects, and is nominally functional.
The ID PROM contains the manufacturing revision level of the IP. If a driver
requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on
which carrier is used. Normally the ID PROM space is directly above the
IPs I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM
automatically.

Standard data in the ID PROM on the IP-Parallel-HV-Mlr is shown in the
figure below. For more information on IP ID PROMs refer to the IP Module
Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-Parallel-HV board will be recorded with a
new code in the DRIVER ID location. -Mlr is set to 0x03 with a customer
number of 0x08.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($04)
0D	Revision	($A0)
0F	reserved	($08)
11	Driver ID, low byte	($03)
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($DD)

FIGURE 8   IP-PARALLEL-HV-MLR ID PROM

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-Parallel-HV-Mlr. Pins marked n/c below are defined by the specification, but not used on the IP-Parallel-HV-Mlr. Also see the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		n/c		5		30	
	D2		MEMSEL*		6		31
D3		n/c		7		32	
	D4		INTSEL*		8		33
D5		n/c		9		34	
	D6		IOSEL*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		INTREQO*		17		42	
	D14		A4		18		43
D15		n/c		19		44	
	BSO*		A5		20		45
BS1*		n/c		21		46	
	n/c		n/c		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		GND		25		50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 9   IP-PARALLEL-HV-MLR LOGIC INTERFACE

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IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-Parallel-HV-Mlr. Also see the User Manual for your carrier board for more information.

Signal	Signal	Pin	Pin
n/c	n/c	1	26
n/c	n/c	2	27
n/c	n/c	3	28
n/c	n/c	4	29
n/c	n/c	5	30
n/c	n/c	6	31
n/c	n/c	7	32
n/c	n/c	8	33
n/c	n/c	9	34
n/c	n/c	10	35
n/c	n/c	11	36
n/c	n/c	12	37
TXDATA	RXDATA	13	38
n/c	AUXDIN_0	14	39
n/c	AUXDIN_1	15	40
n/c	AUXDIN_2	16	41
n/c	n/c	17	42
n/c	n/c	18	43
n/c	n/c	19	44
n/c	n/c	20	45
n/c	n/c	21	46
n/c	n/c	22	47
n/c	n/c	23	48
n/c	n/c	24	49
n/c	GND	25	50

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 10   IP-PARALLEL-HV-MLR IO INTERFACE

TX refers to transmit and RX refers to receive relative to the IP-Parallel-HV-Mlr board. N/C refers to unconnected pins or pins connected to active devices not used in this implementation. Most carriers connect the IP IO 1:1 to the connectors on the carrier. Please check with your carrier for connector mapping.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the IP-Parallel-HV-Mlr when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. It is better design practice to keep the voltage offsets minimized and the potential for current flowing though un-powered electronics to a minimum.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The IP-Parallel-HV-Mlr does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within .7 volts of ground potential.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-Parallel-HV-Mlr is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat dissipation. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-Parallel-HV design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
Internet Address support@dyneng.com

Specifications

Logic Interface: IP Module Logic Interface

Serial Interface: TTL TX Data, RX Data, Three auxiliary TTL inputs.

TX Data rates generated: 250 KHz derived from 32 MHz Oscillator

Software Interface: Control Registers, ID PROM, Vector Register, Status Ports, FIFOs

Initialization: Hardware Reset forces all registers to 0 except the Vector Register which resets to 0XFF.

Access Modes: Word in IO Space (see memory map)
Word in ID Space
Word or LW in Memory space
Vectored interrupt

Access Time: Back-to-back cycles in 500ns (8MHz.) or 125 nS (32 MHz.)

Wait States: 1 to ID or INT space, 2 to IO or MEM space

Interrupt: Tx interrupt at end of transmission
Rx interrupt when data received
Tx FIFO programmable Almost Empty
Rx FIFO programmable Almost Full
Rx FIFO overflow
Rx loss-of-signal

DMA: No Logic Interface DMA Support implemented at this time
Memory space non-compelled supported to FIFOs.

Onboard Options: All Options are Software Programmable

Interface Options: 50 pin flat cable
50 screw terminal block interface
User cable

Dimensions: Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches

Construction: FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.

Temperature Coefficient: 0.89 W/^{o}C for uniform heat across IP

Power: Max. **220** mA @ 5V

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Order Information

IP-Parallel-HV-Mlr

IP Module with 1 Tx and 1 Rx serial channel,
Miller protocol support,
TTL driver and receivers
16 bit IP interface

Tools for IP-Parallel-HV-Mlr

IP-Debug-Bus - IP Bus interface extender
http://www.dyneng.com/ipdbgbus.html
IP–Debug-IO - IO connector breakout
http://www.dyneng.com/ipdbgio.html
HDRterm50 50 position terminal block breakout
from ribbon cable
http://www.dyneng.com/HDRterm50.html

Eng Kit– IP-Parallel-HV-Mlr

IP-Debug-IO - IO connector breakout
IP-Debug-Bus - IP Bus interface extender
Technical Documentation,
    1. IP-Parallel-HV Schematic
    2. IP-Parallel-HV-Mlr Reference test software
Data sheet reprints are available from the
manufacturer's web site
reference software.

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