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User Manual
IP-Parallel-BA1
Digital Parallel Interface IP Module "IP-Tape"

Revision A1
Corresponding Hardware: Revision 01

IP-Parallel-BA1

Digital Parallel Interface
IP Module

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Manual Revision A. Revised 1/31/01

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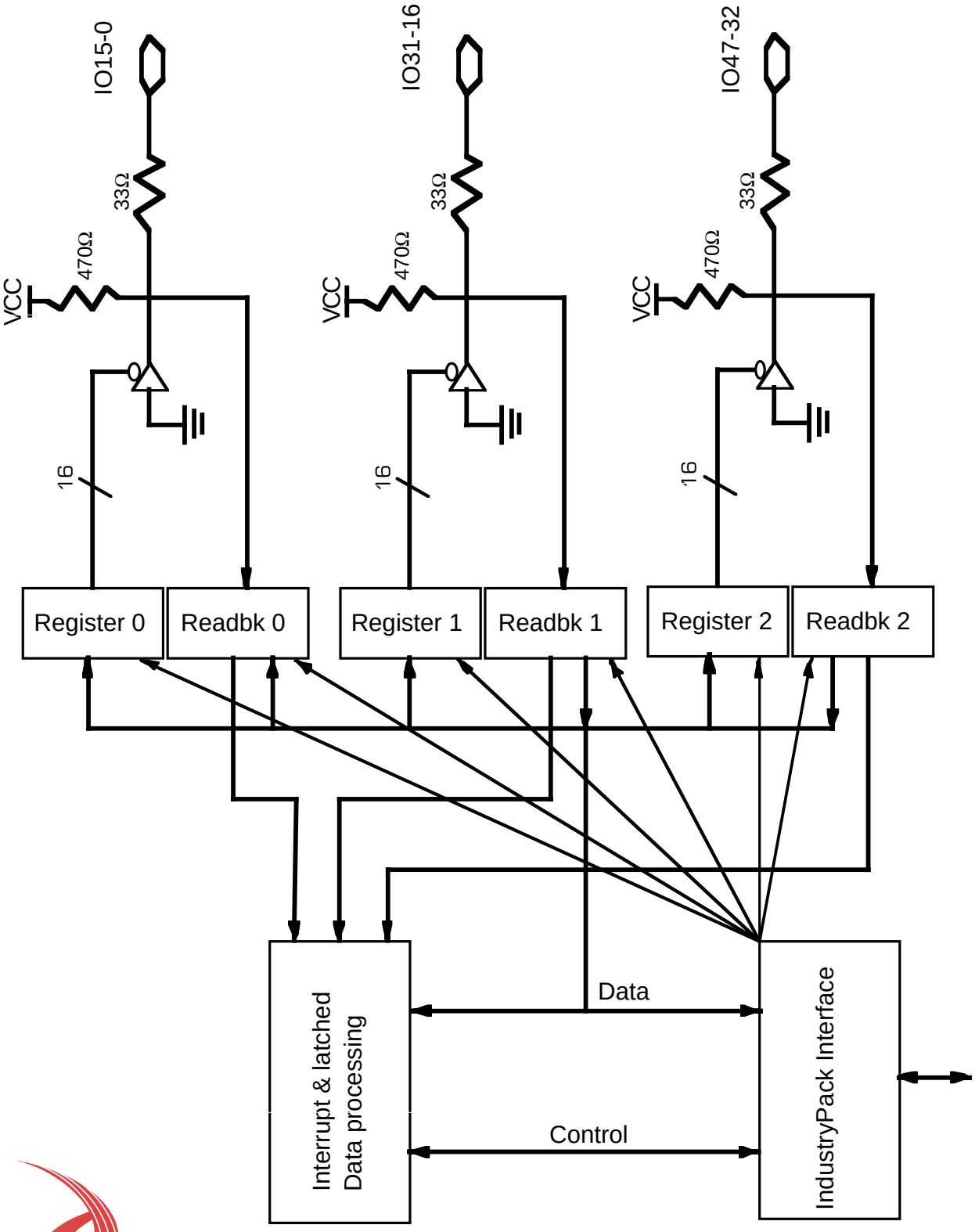
Product Description and Operation



IP-Parallel-BA1 is part of the IP Module family of modular I/O components. The IP-Parallel-BA1 is a customer specific version of the IP-Parallel-IO. With the –BA1 configuration the base board is the same as the –TTL The PROM is re-programmed with a new algorithm to create a “tape” interface.

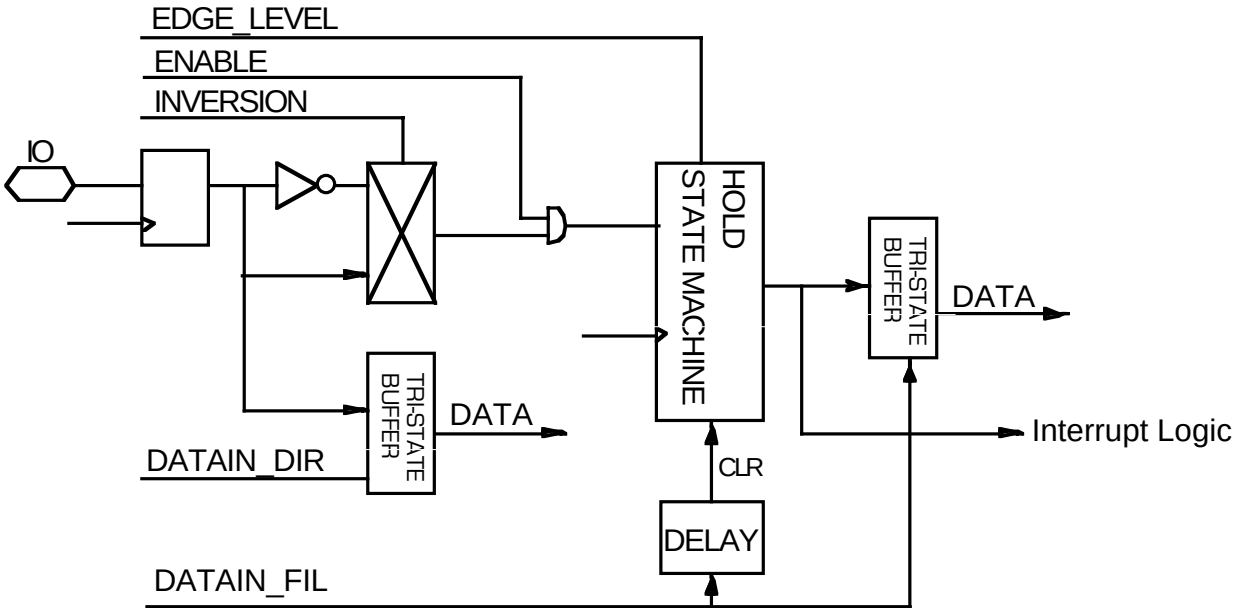
The 48 IO are dedicated to specific purposes with this implementation. The lower 22 IO are always driven bits with the address [21-0]. The next 17 bits are for data and parity. The data and parity are bi-directional. When the bus is not in a write cycle the controls are forced to 0x1ffff for this portion of the bus to turn off the associated open-drain drivers. The data bits are pulled-up to create an 0xFFFF condition on the data bus when it is not driven. The next 4 bits are used for control and are always driven. ENABLEn, DTC_DECn, DTC_ENA, RW are the controls. DTC_DECn is a top level enable and signal that a transaction with the external hardware is in progress. ENABLEn is an active low address enable. DTC_ENA is an active high data enable. RW is hi for read and low for write. The last 5 signals are used for status and are user assigned. For specific pin assignments please see the connector section.

The interface to the tape unit is rather slow. Accesses from the host intended to write to the tape unit are responded to with 1 wait state from the IP. A Busy bit is set in the status register. When the transfer is really completed [several microseconds later] the Busy bit will be cleared. The software can poll the Busy bit to see when the next transfer can occur. Alternately the data filters can be set-up and an interrupt generated when the control signals terminate. Similarly, when a read occurs the IP responds with 1 wait state back to the host. The data read should be discarded. When the data is really available the Busy bit will be cleared. The data read is stored into a register accessible from the IO space.

Each IO line is also brought into the FPGA [Xilinx SpartanXL40]. The IO lines are available as a direct read or after filtering. The data read from the IO will match the register bits if there are no other drivers in the system. The IO bits may not match if another driver is attached.

Each channel has an enable, sense, and edge or level bit associated with it. The enable will block or enable a particular channel from being received into the filtered logic. The sense will either keep the current version or invert the data received. The edge or level control will make the hold circuit wait for an edge from 0 > 1 or react to a level. The hold circuit captures data and holds it until read. The data is registered at the chip edge and then again after the enable and inversion circuitry. Each channel has a separate hold circuit. If a signal is detected to be high then the signal is held until the data is read. With the inversion capability each channel can be programmed to “be high” or to transition to a high condition when the channel has something of interest. The registers are referenced to the IP clock and operate at 8 or 32 MHz depending on the slot configuration. Each group of 16 channels has a separate read clear signal. The

channels can be read in any order and not loose data. The circuit will capture pulses down to 2 reference clocks wide. 60 nS or 250 nS with the standard IP reference clock.



The active high signals are combined to create an interrupt request based on the captured and held data. If the master interrupt enable is “enabled” then the interrupt is passed onto the system. The interrupt is cleared by reading the data or disabling the master enable. The user can program each channel to use the edge or level condition. The edge is particularly useful for long duration signal where repeated interrupts are not desired. The alternate approach is to flip the sense bit and create an interrupt when the signal has switched to the opposite polarity. Instruction order is important. Once the interrupt is detected the sense needs to be switched before the interrupt is re-enabled or a second interrupt is likely to be generated.

With each IO line having all three controls plus independent direction a lot of control possibilities exist.

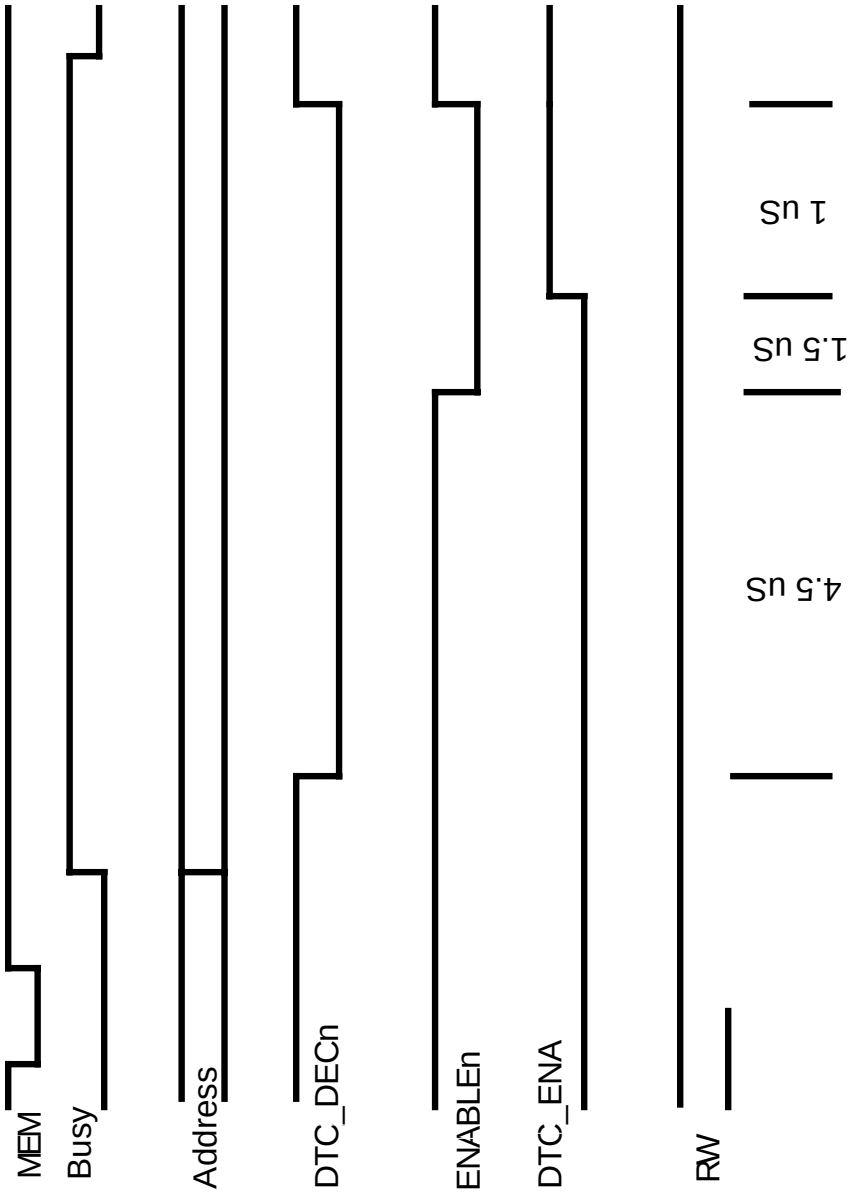
In addition to the BA1 version, other custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there, we will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please contact Dynamic Engineering with your custom application. Several of the IO bits are implemented on the long line clock pins of the FPGA. External clock references can be designed in as a custom option. There is a user oscillator position to support custom state machines and IO requirements. The DMA

controls, second interrupt level, and memory space controls are routed to the FPGA to allow for future upgrades.

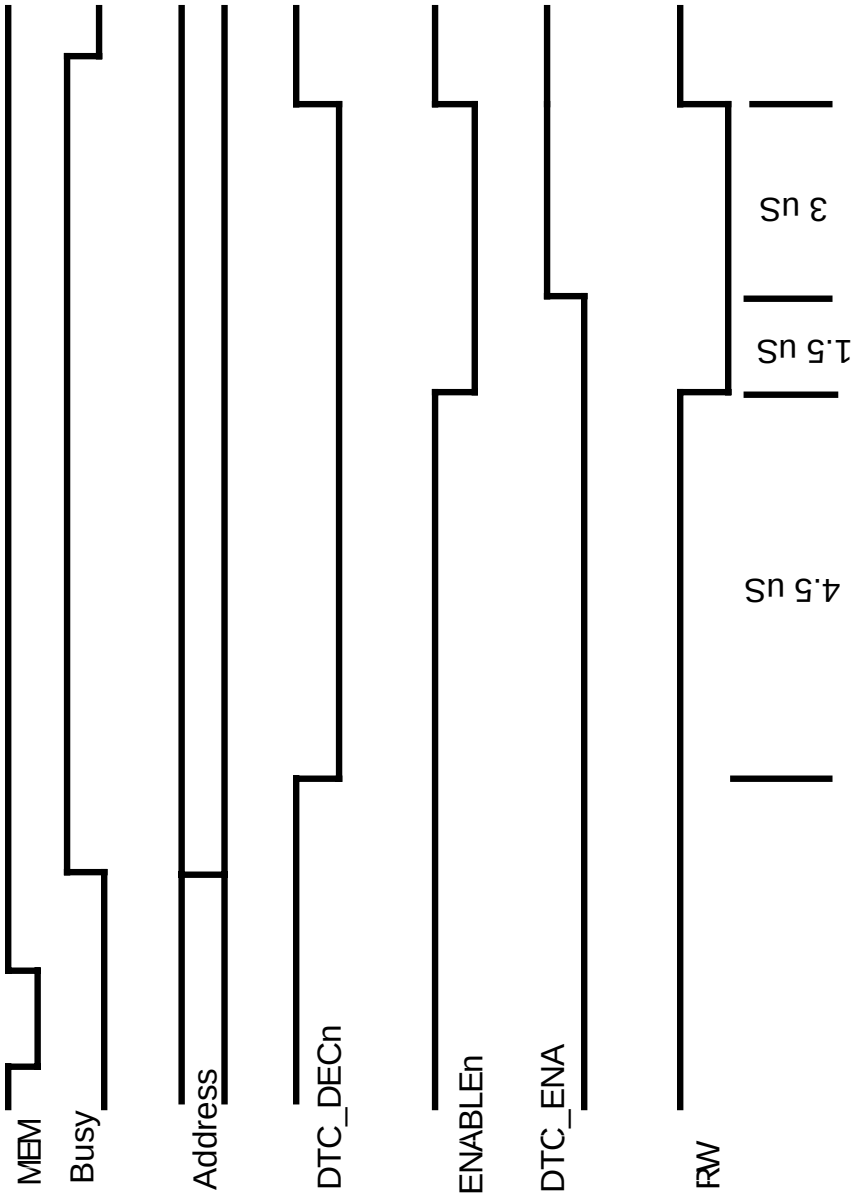
The IP-PARALLEL-BA1 supports both 8 and 32 Mhz. IP Bus operation. All configuration registers support read and write operations for maximum software convenience. Word operations are supported (please refer to the memory map). The ID, IO, MEM and INT spaces are utilized by the IP-Parallel-BA1 design.

The IP-PARALLEL-BA1 conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. The PCI3IP card makes a convenient development platform in many cases. http://www.dyneng.com/pci_3_ip.html

Interrupts are supported by the IP-PARALLEL-BA1. The interrupt occurs when a programmed transition occurs. The interrupts are individually maskable – each IO channel has a separate mask. The vector is user programmable by a read/write register. The interrupt occurs on IntReqO. The vector can be read in the IO space or automatically with the INT space.



The Timing diagram is for a Read access from the Tape unit. The cycle starts with a Memory Space access and continues until the data is stored several uS later. Busy indicates that the transfer is active. The IP response happens with a 1 wait-state delay.



The Timing diagram is for a Write access from the Tape unit. The cycle starts with a Memory Space access and continues until the data is stored several uS later. Busy indicates that the transfer is active. The IP response happens with a 1 wait-state delay. Notice that the cycle time is longer than for a read cycle.

The delays are programmable within a state-machine. With minimal effort the delays can be changed to alternate values.

Address Map

Function		Offset	Width	Type
cntl0	EQU	$00	word	read/write
cntl1	EQU	$02	word	read only this version
cntl2	EQU	$04	word	NA this version
Base_cntl	EQU	$06	word	read/write
Int En0	EQU	$08	word	read/write
Int En1	EQU	$0A	word	read/write
Int En2	EQU	$0C	word	read/write
vector	EQU	$0E	word	read/write
Int EdgLvl0	EQU	$10	word	read/write
Int EdgLvl1	EQU	$12	word	read/write
Int EdgLvl2	EQU	$14	word	read/write
Int Pol0	EQU	$18	word	read/write
Int Pol1	EQU	$1A	word	read/write
Int Pol2	EQU	$1C	word	read/write
status	EQU	$1E	word	read -
dat_in_fil0	EQU	$20	word	read
dat_in_fil1	EQU	$22	word	read
dat_in_fil2	EQU	$24	word	read
dat_in_dir0	EQU	$28	word	read
dat_in_dir1	EQU	$2A	word	read
dat_in_dir2	EQU	$2C	word	read
Memory Space			word	read/write
IDPROM			byte on word boundary	read

FIGURE 1 IP-PARALLEL-BA1 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-PARALLEL-BA1. The addresses are all offsets from a base address. The carrier board that the IP is installed into provides the base address.

Programming

Programming the IP-PARALLEL-BA1 requires the ability to read and write data in the host's I/O and Memory space. The base address is determined by the IP Carrier board.

In order to receive data from the IO, the software is only required to read from the "Direct" port. Alternatively the filtered data path can be programmed with the enable, Level and edge and then the Filtered data used. If desired, the interrupt can be enabled and the interrupt vector written to the vector register. Each of the IO will reflect the value of the IO line at the time. When an access to the tape machine is needed then the memory space access should be used.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example, $40 is a valid user vector for the Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the mask should be set. The Level and Edge conditions programmed then the enables set to receive data. The incoming data can be pulsed. The hardware will hold any pulse or level detected until the data is read by the software.

Data is written to the Control [cntl] registers. Any active low bits are used to enable the open drain drivers. The drivers have 64 mA sink capability and overcome the pull-up [10 mA] to create a '0' on the bus. A '1' in a bit position turns off the driver leaving the pull-up to set the level to a '1'. Other hardware in the system can also pull the signal line to '0'. If enabled the lines which are controlled by the outputs can cause interrupts back to the host. Usually these will be disabled to prevent self interrupting.

When 485 transceivers are installed the driver section creates a differential signal pair. The pull-up resistors are not installed.

A 32 bit write/read with some CPUs will result in two 16 bit accesses to the hardware with automatic incrementing addresses. The 32 bit access is quite a bit faster than a software loop. The PCI3IP is an example of a carrier that supports 32 bit to 16 bit mapping automatically. The lower 32 bits of the output, "data in filtered", and "data in direct" are on long word boundaries to utilize this feature if available. [http://www.dyneng.com/pci_3_ip.html]

The –BA1 version has a special interface for interfacing with a tape machine. When an access is made to any address within the Memory Space an access is started. The hardware senses read or write and stores the address used. The address is driven onto the IO port pins. A delay occurs and then the hardware automatically performs the read or write protocol. When the transfer is

completed the Busy bit is cleared [set with Memory Space access] and if a read the data is stored into a register for software access. The Busy bit is located in the status register. An interrupt can be programmed if desired from any of the control bits using the filtered data port.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

Register Definitions

CNTLO

$00 Parallel Control Register Port read/write

CONTROL REGISTER 0	
DATA BIT	**DESCRIPTION**
15-0	clock control register

FIGURE 2 IP-PARALLEL-BA1 CONTROL REGISTER 0 BIT MAP

Set to 0x0000 for 8 MHz. IP clock operation.
Set to 0x6000 for 32 MHz. IP clock operation

CNTL1

$02 Parallel Control Register Port read only

CONTROL REGISTER 1	
DATA BIT	**DESCRIPTION**
15-0	captured data read back

FIGURE 3 IP-PARALLEL-BA1 CONTROL REGISTER 1 BIT MAP

After a Memory Space read, the data is stored into this port

CNTL2

$04 Parallel Control Register Port read/write

CONTROL REGISTER 2	
DATA BIT	**DESCRIPTION**
15-0	

FIGURE 4 IP-PARALLEL-BA1 CONTROL REGISTER 2 BIT MAP

Unimplemented and unused in this version. An access will not return useful data.

Base_CNTL

$06 BISERIAL Control Register Port read/write

CONTROL REGISTER BASE

DATA BIT	DESCRIPTION
15-6	spare
5	Read Parity 1 = odd, 0 = even
4	Write Parity 1 = odd, 0 = even
3	spare
2	force interrupt 1 = force
1	master interrupt enable 1 = enabled
0	spare

FIGURE 5 IP-PARALLEL-BA1 BASE CONTROL REGISTER BIT MAP

1. INT_EN is the master interrupt enable. Default is 0. If set to 1 then if one or more of the filtered input data conditions is met an interrupt will be generated on level 0.

2. Force Interrupt is used to create an interrupt for test and software development purposes. Set the bit to cause an interrupt and clear the bit to remove the interrupt. The I0 bits can be used for the same purpose if the filter controls are properly set. Requires INT_EN to be enabled.

4,5 Parity control bits. When set to '1' the Parity generated or checked for is odd. When set to '0' the Parity generated or checked for is even. Odd means that the parity bit will be set or not to create an odd number of 1's within the data plus parity word. For example: 0x1234 has 5 ones, with odd parity selected the parity bit would be '0' for a write or checked against a '0' for a read. Parity errors are reported in the status register.

INTerrupt Enable

Int_en0 $08 Parallel Control Register Port read/write

Interrupt Enable	
DATA BIT	**DESCRIPTION**
15-0	int_en 15-0 Interrupt Enable 1 = enabled, 0 = disabled

FIGURE 6 IP-PARALLEL-BA1 INTERRUPT ENABLE 0 BIT MAP

Int_en1 $0A Parallel Control Register Port read/write

Interrupt Enable	
DATA BIT	**DESCRIPTION**
15-0	int_en 31-16 Interrupt Enable 1 = enabled, 0 = disabled

FIGURE 7 IP-PARALLEL-BA1 INTERRUPT ENABLE 1 BIT MAP

Int_en2 $0C Parallel Control Register Port read/write

Interrupt Enable	
DATA BIT	**DESCRIPTION**
15-0	int_en 47-32 Interrupt Enable 1 = enabled, 0 = disabled

FIGURE 8 IP-PARALLEL-BA1 INTERRUPT ENABLE 2 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is enabled to be a potential interrupter and to be captured by the hold circuit. The enable is applied after the inversion control.

INTerrupt Edge_Lvl

Edg_Lvl 0 $10 Parallel Control Register Port read/write

EDGE_LVL	
DATA BIT	**DESCRIPTION**
15-0	Edg_Lvl 15-0 1 = edge, 0 = level

FIGURE 9 IP-PARALLEL-BA1 INTERRUPT EDG_LVL 0 BIT MAP

Edg_Lvl 1 $12 Parallel Control Register Port read/write

EDGE_LVL	
DATA BIT	**DESCRIPTION**
15-0	Edg_Lvl 31-16 1 = edge, 0 = level

FIGURE 10 IP-PARALLEL-BA1 INTERRUPT EDG_LVL 1 BIT MAP

Edg_Lvl 2 $14 Parallel Control Register Port read/write

EDGE_LVL	
DATA BIT	**DESCRIPTION**
15-0	Edg_Lvl 47-32 1 = edge, 0 = level

FIGURE 11 IP-PARALLEL-BA1 INTERRUPT EDG_LVL 2 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is captured only if there is a transition from '0' to '1'. If set to '0' then anytime the IO line is detected to be '1' the hold circuit will be set. The hold circuit will retain the data until read by the corresponding data_in_fi(x) is accessed. The hold circuits are after the enable and inversion in the pipeline.

INTerrupt Polarity

Pol 0 $18 Parallel Control Register Port read/write

DATA BIT	Polarity DESCRIPTION
15-0	POL 15-0 1 = invert, 0 = not inverted

FIGURE 12 IP-PARALLEL-BA1 INTERRUPT POL 0 BIT MAP

Pol 1 $1A Parallel Control Register Port read/write

DATA BIT	Polarity DESCRIPTION
15-0	POL 31-16 1 = invert, 0 = not inverted

FIGURE 13 IP-PARALLEL-BA1 INTERRUPT POL 1 BIT MAP

Pol 2 $1C Parallel Control Register Port read/write

DATA BIT	Polarity DESCRIPTION
15-0	POL 47-32 1 = invert, 0 = not inverted

FIGURE 14 IP-PARALLEL-BA1 INTERRUPT POL 2 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is inverted. If set to '0' then no inversion is applied.

Data Input Filtered

Datain_fil0 $20 Parallel Control Register Port read/write

Filtered Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_FIL 15-0

FIGURE 15 IP-PARALLEL-BA1 DATAIN_FILO BIT MAP

Datain_fil1 $22 Parallel Control Register Port read/write

Filtered Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_FIL 31-16

FIGURE 16 IP-PARALLEL-BA1 DATAIN_FIL1 BIT MAP

Datain_fil2 $24 Parallel Control Register Port read/write

Filtered Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_FIL 47-32

FIGURE 17 IP-PARALLEL-BA1 DATAIN_FIL2 BIT MAP

The data bits correspond to the IO lines after the filters have been applied. The data remains latched until the register is read. The three registers are independent for reading and clearing purposes. Read [clear] the registers after any control change to insure that no false positives are reported.

Data Input Direct

Datain_dir0 $28 Parallel Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_DIR 15-0

FIGURE 18 IP-PARALLEL-BA1 DATAIN_DIR0 BIT MAP

Datain_dir1 $2A Parallel Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_DIR 31-16

FIGURE 19 IP-PARALLEL-BA1 DATAIN_DIR1 BIT MAP

Datain_dir2 $2C Parallel Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_DIR 47-32

FIGURE 20 IP-PARALLEL-BA1 DATAIN_DIR2 BIT MAP

The data bits correspond to the IO lines without filters being applied. The data is a direct reflection of the current state of the IO lines. Metastable protection registers are in place but no hold registers.

Status

Status $1E Parallel-BA1 Status Register Port read only

Direct Data	
DATA BIT	**DESCRIPTION**
15-2	unused mask off.
1	Parity read status 1 = good
0	Busy Bit 1= busy

FIGURE 21 IP-PARALLEL-BA1 STATUS BIT MAP

The Busy Bit is set when a read or a write access to the IP happens in the Memory space. The event triggers an access to the tape unit. The access is quite long relative to standard IP accesses. The Host is released early and the Busy Bit used to indicate completion of the transfer. When low the data has been written to the tape unit or the data is stored into the holding register.

The Parity status for a read access is stored into bit 1. The status is updated with each read from the tape unit. If the calculated parity matches the stored parity then a '1' results and if the parity does not match a '0' is reported.

BIS_VECTOR

$0E Parallel Interrupt Vector Port

The Interrupt vector for the IP-Parallel-BA1 is stored in this byte wide register. This read/write register is initialized to 'xxFF' upon power-on reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered. The interrupt is automatically cleared when the CPU acknowledges the interrupt.

Interrupts

All IP Module interrupts are vectored. The vector from the IP-PARALLEL-BA1 comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-PARALLEL-BA1 state machines generate an interrupt request when a programmed condition is detected on the IO lines. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will

automatically supply the appropriate interrupt vector and clear the request when accessed by the CPU. The source of the interrupt is obtained by reading DATA_IN_FILO-2. The status remains valid until the registers are read. The interrupt status is auto-cleared when the registers are accessed.

Some carrier boards pre-fetch data. If your carrier board pre-fetches the interrupt status, then the status may be cleared when the SW goes to look at it. If this is an issue then be careful with the order of reading the registers to prevent the pre-fetching function from affecting operation.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BASE_CNTL register. The individual enables for IO lines are controllable through INT_ENO-2. The enable operates before the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to read the holding register [DATAIN_FILO-2], reset the board, or disable the interrupt. The Interrupt acknowledge cycle fetches the vector, but does not clear the interrupt request in this design.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision to be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-PARALLEL-BA1 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-Parallel-BA1 board will be recorded with a new code in the DRIVER ID and reserved fields.

Address	Data	BA1
01	ASCII "I"	$49
03	ASCII "P"	$50
05	ASCII "A"	$41
07	ASCII "H"	$48
09	Manufacturer ID	$1E
0B	Model Number	$03
0D	Revision	$A0
0F	reserved	$01
11	Driver ID, low byte	$01
13	Driver ID, high byte	$00
15	No of extra bytes used	$0C
17	CRC	$8D

FIGURE 22 IP-PARALLEL-BA1 ID PROM

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-PARALLEL-BA1. Pins marked n/c below are defined by the specification, but not used on the IP-PARALLEL-BA1. Also see the User Manual for your carrier board for more information.

GND		GND	1	26	
	CLK	+5V	2		27
Reset*		R/W*	3	28	
	D0	IDSEL*	4		29
D1		DMAReq0*	5	30	
	D2	MEMSEL*	6		31
D3		DMAReq1*	7	32	
	D4	IntSel*	8		33
D5		DMAck*	9	34	
	D6	IOSel*	10		35
D7		n/c	11	36	
	D8	A1	12		37
D9		DMAEnd*	13	38	
	D10	A2	14		39
D11		n/c	15	40	
	D12	A3	16		41
D13		IntReq0*	17	42	
	D14	A4	18		43
D15		IntReq1*	19	44	
	BS0*	A5	20		45
BS1*		n/c	21	46	
	n/c	A6	22		47
n/c		Ack*	23	48	
	+5V	n/c	24		49
GND		GND	25	50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 23 IP-PARALLEL-BA1 LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-BA1. Pins marked. Also see the User Manual for your carrier board for more information.

IO_0	IO_24		1	26	
IO_1		IO_25	2		27
IO_2	IO_26		3	28	
IO_3		IO_27	4		29
IO_4	IO_28		5	30	
IO_5		IO_29	6		31
IO_6	IO_30		7	32	
IO_7		IO_31	8		33
IO_8	IO_32		9	34	
IO_9		IO_33	10		35
IO_10	IO_34		11	36	
IO_11		IO_35	12		37
IO_12	IO_36		13	38	
IO_13		IO_37	14		39
IO_14	IO_38		15	40	
IO_15		IO_39	16		41
IO_16	IO_40		17	42	
IO_17		IO_41	18		43
IO_18	IO_42		19	44	
IO_19		IO_43	20		45
IO_20	IO_44		21	46	
IO_21		IO_45	22		47
IO_22	IO_46		23	48	
IO_23		IO_47	24		49
GND	GND		25	50	

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 24 IP-PARALLEL-BA1 IO INTERFACE

-BA1 signals	IO Number
Address 21-0	IO_21-0
Data 15-0	IO_37-22
Parity	IO_38
DTC_DECn	IO_39
DTC_ENA	IO_40
RW	IO_41
ENABLEn	IO_42
Status inputs	IO_47-43 -> read through data_dir2 or data_fil2

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the IP-PARALLEL-BA1 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within .7 volts of ground potential.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails.
[http://www.dyneng.com/HDRterm50.html]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-PARALLEL-BA1 is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required. *Please order standard mounting kit for IPs if you want this option*. [IP-MTG-KIT]

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-Parallel-BA1 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering

435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
e-mail support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Parallel Interface:	Up to 48 open drain IO. 64 mA sink with 10 mA pull-up Up To 24 RS485 Transceivers
Software Interface:	Control Registers, ID PROM, Vector Register, Status Ports
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	Word I/O Space (see memory map) Word in ID Space Vectored interrupt
Access Time:	back-to-back cycles in 500ns (8Mhz.) or 125 nS (32 Mhz.)
Wait States:	1 to all spaces
Interrupt:	Multiple interrupt filtering options available on each IO line. Enabled, Active hi or low, edge or level.
DMA:	No Logic Interface DMA Support implemented at this time.
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface [HDRterm50] User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{0}C for uniform heat across IP
Power:	Max. **TBD** mA @ 5

Order Information

The IP-Parallel-BA1 board has 7 standard configurations.
http://www.dyneng.com/ip_parallel_io.html

"**-TTL**"	IP Module with 48 TTL IO open drain drivers with 470Ω pull-up 16 bit IP interface
"**-1**"	40 TTL and 4-485
"**-2**"	32 TTL and 8 - 485
"**-3**"	24 TTL and 12 - 485
"**-4**"	16 TTL and 16 – 485
"**-5**"	8 TTL and 20 – 485
"**-485**"	24 – 485
"**-BA1**"	48 TTL lines, 22 Address, 16 Data, 1 Parity, 4 Control out, 5 Status inputs

Tools for IP-PARALLEL-BA1

IP-Debug-Bus - IP Bus interface extender with testpoints, isolated power and quickswitch technology to allow hot swapping of IPs or power cycling without powering down the host.
http://www.dyneng.com/ipdbgbus.html

IP-Debug-IO II - IndustryPack IO connector breakout with testpoints, ribbon cable headers, and locations for user circuits. http://www.dyneng.com/ipdbgio.html

HDRterm50 - Ribbon cable compatible 50 pin header to 50 screw terminal header. Comes with DIN rail mounting capability. http://www.dyneng.com/HDRterm50.html

PCI3IP - 1/2 length PCI card with 3 IP slots.
http://www.dyneng.com/pci_3_ip.html

IP-MTG-KIT – 4 metric stainless screw and stand-off pairs to retain IP-Parallel-BA1 against the carrier board. Flat head screws match IP Specification mounting requirements.