DYNAMIC ENGINEERING
435 Park Dr., Ben Lomond, Calif. 95005
831-336-8891 **Fax** 831-336-3840
http://www.dyneng.com
sales@dyneng.com
Est. 1988

User Manual

IP-BiSerial-RTN2

Bi-directional Serial Data Interface IP Module

Revision A
Corresponding Hardware: Revision A

IP-BiSerial-RTN2
Bi-directional Serial Data Interface
IP Module

Dynamic Engineering
435 Park Drive
Ben Lomond, CA 95005
831- 336-8891
831-336-3840 FAX
www.dyneng.com

Manual Revision A. Revised Jan 19th, 2001

Table of Contents

List of Figures

Product Description

IP-BISERIAL-RTN2 is part of the IP Module family of modular I/O components. The IP-BISERIAL-RTN2 is capable of providing multiple serial protocols. The standard protocol implemented provides a Data, Clock and Strobe interface with Ready control. The -RTN2 version is a custom modification. The main modifications include switching to lsb first format, adding parity generation and checking.

In addition to the RTN2 version other custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there we will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a "standard" special order product. Please contact Dynamic Engineering with your custom application.

The IP-BISERIAL-RTN2 supports both 8 and 32 Mhz. IP Bus operation. The IP Clock or an external reference is used to derive the reference clocks for the serial operation. Please be sure to select the proper clock divisors and source selector after reset to insure proper operation. Please refer to the programming section for details.

Both single ended and differential I/O are available on the serial signals. The differential drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are terminated with 180Ω. The single ended driver signal is characterized as an open drain driver with 24 mA of sink. For convenience A 2KΩ pull-up is supplied on board, for faster termination a second pull-up can be added at the receiving end of the circuit. Single ended signals are received through 33Ω resistors. Care should be taken with the single ended signals. Transients can damage the board.

All configuration registers support read and write operations for maximum software convenience. Word and byte operations are supported (please refer to the memory map).

The IP-BISERIAL-RTN2 conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one.

The serial channels are supported by an 8K by 16 bit FIFO. The FIFO supports word accesses. A write path exists for loop-back testing. The serial receive channel looks for data in 16 bit transfers plus programmable parity. The received words are then loaded into the FIFOs. The data length loaded is determined by the strobe signal. The host can poll or wait for the message complete interrupt. The message can be read directly from the input FIFO.

The Output channel has a separate 8k x 16 FIFO. The FIFO supports word accesses. Programmable parity is automatically generated and appended to each data word. The FIFO can be accessed directly for loop back testing.

The IP-BISERIAL-RTN2 utilize several clock sources. The IP clock, reference oscillator, or user input clock can be clock sources. A programmable divider creates multiple clock rates from the base rate. Please refer to the clock selection section within the programming section for details.

Interrupts are supported by the IP-BISERIAL-RTN2. The interrupt occurs at the end of the transmission whether data is received or sent or both. The programmable interrupts are available to provide an almost empty indicator for TX and almost full indicator for RX. The interrupts are individually maskable. The vector is user programmable by a read/write register. The interrupt occurs on IntReq0. The FIFO status is available for the FIFO making it possible to operate in a polled mode.

Theory of Operation

The IP-BISERIAL-RTN2 is designed for the purpose of transferring data from one point to another with a serial protocol.

The IP-BISERIAL-RTN2 features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BISERIAL design. Only the drivers, receivers, boot PROM and FIFOs are external to the Xilinx device.

The IP-BISERIAL-RTN2 is a part of the IP Module family of modular I/O products. It meets the IP Module Vita Standard. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design. In standard configuration it is a Type 1 mechanical with no components on the back of the board and one slot wide.

The bus interface to the host CPU is controlled by a logic block within the Xilinx device that contains the decoding and timing elements required to interface to the IP bus interface. The timing is referenced to the 8 or 32 MHz IP logic clock. The IP responds to the ID, INTSEL, MEM and IO selects. The DMA control lines are connected to the Xilinx for future revisions, and are not used at this time. The BISERIAL design requires wait states for read or write cycles to any address. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host removes the SEL line. Local timing terminates a write cycle prior to the SEL being deasserted. If no hold cycles are requested by the host, the IP-BISERIAL-RTN2 is capable of supporting 16+ MB per second data transfer rate with a 32 Mhz. reference rate.

The serial I/O can support many protocols. The -RTN2 timing is shown in the next diagram. The clock is free running, the data is valid on the falling edge of the clock, and strobe frames the data. The timing is in reference to an external user supplied clock. The clock is input on the TX_RDY differential receiver line pair. The TX state-machine synchronizes the output transmission to this clock. There are small delays associated with receiving the external clock through the differential receiver and bringing the signal into the FPGA. The internal version of the clock is also re-transmitted on the reference clock output. The RX function receives data using the clock on the TX RDY.

A pair of state machines within the FPGA control all transfers between the FIFO and FPGA, and the FPGA and the data buffers. The TX state machine reads from the transmit FIFOs and loads the shift registers before sending

the data. The Rx state machine receives data from the data buffers and takes care of moving data from the shift register into the Rx FIFO.

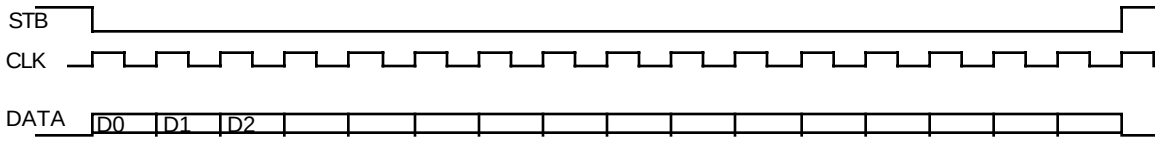

FIGURE 1 IP-BISERIAL-RTN2 SERIAL PROTOCOL TIMING

When the start bit is detected high to begin the transfer, the data is read from the TX FIFO and loaded into the shift register. The LSB is then present at the output of the data buffer. The Strobe is activated at the same time. One half clock period later the Falling edge of the data clock is driven to the output clock buffer. One half clock period later the data is transitioned to the next value. The LSB+1 is now on the data lines. The process repeats until the first word is transferred. At the end of the word a 17th bit can be added for parity. The parity bit is programmable to be odd or even. Assuming that there is data to be sent in the FIFO a second word is read and loaded into the shift register and sent out onto the bus. The process is repeated until that word is transferred. The transfer will continue until the FIFO is empty when it is time to load. The data stream is continuous.

The receive function is similar. When the Strobe is detected low, data is loaded into the receive shift register on the falling edge of the data clock. Once a word has been received the data is loaded into the receive FIFO. When the strobe goes inactive the transfer has been completed and an interrupt is generated to the host [if enabled]. The receiver checks for parity, over-run and framing errors. If an error is detected the appropriate bit in STAT1 is set.

A counter keeps track of the number of words received. The counter counts once per word received. The counter loads the count into a latch and then clears the counter to allow a second message to be received before the count is read. The count self clears when read through STAT2. The counter is 13 bits wide. An error is detected if the received count is not read before it is time to update the stored count. The update occurs at the end of a message. The time to read is the length of the next message to be received and is system dependent. The data is still in the FIFO even if the count is not read. The count will not reflect the total data stored in this case.

Address Map

Function		Offset	Width	Type
BIS_CNTLO	EQU	$00	byte on word boundary	read/write
BIS_CNTL1	EQU	$02	byte on word boundary	read/write
BIS_CNTL2	EQU	$04	byte on word boundary	read/write
BIS_CNTL3	EQU	$16	word	
BIS_VECTOR	EQU	$06	byte on word boundary	read/write
BIS_STATO	EQU	$08	byte on word boundary	read
BIS_STAT1	EQU	$0A	byte on word boundary	read
BIS_STAT2	EQU	$0C	word on word boundary	read
BIS_FTX_W	EQU	$10	word	write
BIS_FTX_R	EQU	$22	word	read
BIS_FRX_W	EQU	$20	word	write
BIS_FRX_R	EQU	$40	word	read
BISERIAL_IDPROM	EQU	$80	byte on word boundary	read

FIGURE 2 IP-BISERIAL-RTN2 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-BISERIAL-RTN2. The addresses are all offsets from a base address. The carrier board that the IP is installed into provides the base address.

Programming

Programming the IP-BISERIAL-RTN2 requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Carrier board. This documentation refers to the address where the IO space for the slot that the IP is installed in as the base address.

In order to receive data the software is only required to enable the RX state machine, FIFOs, and set the parity properly. If desired, the interrupt can be enabled and the interrupt vector written to the vector register. Data will be loaded into the FIFOs as it is received.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example $40 is a valid user vector for the

Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the mask should be set. When the start bit is set the hardware looks to make sure that the strobe is not active then begins looking for it to be active. In this manner the data received is protected from joining mid-message. Once a new strobe assertion is detected the data loading process begins. When the strobe is detected to be deasserted the interrupt request is asserted to let the host know that the data is available. The software can read the word count and set-up a loop counter to efficiently read the data from the FIFOs. If the next message starts and completes then the FIFO empty flag can be used to control the amount of data to read.

The end of transmission interrupt will indicate to the software that the message has been started and that the message has terminated. If both the TX and RX interrupts are enabled then the SW needs to read BIS_STAT1 to see which source caused the interrupt. Reading BIS_STAT1 will clear the interrupt status, and the INTACK cycle will clear the actual interrupt. The interrupt status can be read after the INTACK cycle. It is a good idea to read the status register to force the RX_INT and TX_INT bits to 0 before Start is enabled to insure that the RX_INT or TX_INT=1 value read by the interrupt service routine came from the current reception.

Before transmitting data the FIFOs are enabled and the data loaded. The RTN-2 design has both internal and external clock selection capability. The baud rate selections are used to select the output rate. The divided version or the base rate can be selected for the reference rate on the TX state machine. The parity bit can be programmed to be odd, even, and on or off. Once the complete message is loaded and the controls set properly the start bit can be set to cause the transfer to begin. If a slow clock rate is selected and a long message is to be sent then data can be loaded during transmission to save operational time. Care must be taken to make sure that the FIFOs do not become empty. When the TX interrupt is received the transmission has been completed and another message can be loaded. All that needs to happen with a second message is to load the FIFO and set the start bit.

Messages longer than 16K bytes can be accommodated by special ordering HW with larger FIFOs or by using the MT and Full flags on the FIFOs to poll during the transfer…fill the tx FIFO and when not full add more data until full. On the receive side poll and when not empty read the data until empty. The PAE and PAF flags are to provide an almost empty interrupt to allow the TX side to operate in an interrupt driven mode with longer messages. Similarly the PAF can be used to provide an almost full

interrupt to the receive side host to allow interrupt driven long message capability.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

Register Definitions

BIS_CNTL0

$00 BISERIAL Control Register Port read/write

CONTROL REGISTER 0	
DATA BIT	**DESCRIPTION**
7	SPARE
6	TX OFF STATE
5	TX PARITY ON/ OFF
4	TX PARITY ODD / EVEN
3	INT FORCE
2	INT EN FAE
1	INT EN TX
0	STRT_TX

FIGURE 3 IP-BISERIAL-RTN2 CONTROL REGISTER 0 BIT MAP

0. STRT_TX is set to send data. The bit is auto cleared at the end of a transmission.

1. INT_EN_TX is the Interrupt Enable bit for the Transmit channel. The default state is off. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the transmission is complete. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.

2. INT_EN_FAE is the Interrupt Enable bit for the Programmable Almost Empty condition. The default state is off. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the FIFO level falls to the almost empty count. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.

3. INT FORCE is used to create an interrupt for test and software development purposes. Set the bit to cause the interrupt and clear the bit

to remove the interrupt. Requires the master interrupt enable to be '1' to have effect.

4. TX Parity ODD / EVEN when '1' selects odd parity and when 'O' selects even parity generation.

5. TX Parity ON / OFF when '1' inserts parity into the data stream at the end of each word for a 17 bit word. When 'O' parity is not inserted for a 16 bit word.

6. TX OFF State defines the level of the data line between transmitted words.

BIS_CNTL1

[$02 BISERIAL Control Register Port read/write

CONTROL REGISTER 1	
DATA BIT	**DESCRIPTION**
7	ENABLE FIFO
6	SPARE
5	RX PARITY ON / OFF
4	RX PARITY ODD / EVEN
3	SPARE
2	INT EN PAF
1	INT EN RX
0	STRT_RX

FIGURE 4 IP-BISERIAL-RTN2 CONTROL REGISTER 1 BIT MAP

0. STRT_RX is used to enable the receive state machine to receive messages. The start bit is auto-cleared at the end of a transmission.

1. INT EN RX is used to enable the receive interrupt. The default is disabled. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the Strobe returns to the off state. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.

2. INT EN PAF is used to enable the Programmable Almost Full interrupt. The default is disabled. If enabled and the master interrupt enable is also enabled then an interrupt is requested when FIFO fills to the almost full condition. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.

4. RX PARITY ODD / EVEN is used to select the expected parity type to be tested for by the RX state machine. 1 = odd, 0 = even.

4. RX PARITY ON / OFF is used to enable parity checking. '1' = parity check and 17 bit data expected. '0' = parity checking disabled and 16 bit data expected.

7. ENABLE FIFO is used to reset the FIFOs. The default state is reset. The FIFOs must be taken out of reset to be used to store data. Please refer to FTX_LD and FRX_LD [control reg 2]. Reset must be set high then low then high while the clock is running to the FIFOs to cause a proper reset with guaranteed flag operation. We suggest using the IP clock as the reference

for this process.

BIS_CNTL2

[$04 BISERIAL Control Register Port read/write

CONTROL REGISTER 2	
DATA BIT	**DESCRIPTION**
7	INT EXT RX CLK
6	Master INT_EN
5	FRX_LD
4	FTX_LD
3	RX_RDY [spare output]
2	Spare
1	spare program to ‘0’
0	RXTTL_422

FIGURE 5 IP-BISERIAL-RTN2 CONTROL REGISTER 2 BIT MAP

0. RX_TTL_422 is the control bit to select whether the data, clock, and strobe should be received as TTL or 422 signals. Default state = 0 = 422 [485] a ‘1’ selects TTL inputs. Set to 0 for BA-2 use.

3. RX_RDY bit is used to set the state of the Receiver Ready Bit. If the system needs Receiver Input Ready control then program the transmitter to output when Ready is ‘1’ and use the RX_RDY to grant or block transmission. Default is ‘0’. Can be used as a general purpose output bit.

4,5. FRX_LD is tied to the RX FIFO WE2/_LD pin. FTX_LD is tied to the TX FIFO WE2/_LD pin.When the FIFOs are taken out of reset it is possible to set-up the FIFO to accept commands to program the way the programmable almost empty and programmable almost full signals operate. ***In the standard transfer mode these pins are set hi before CLR_FIFO is released to use as a second WE control pin***. If the PAE and PAF flags are used at a different than default debth then the flags will require programming. The default is 7 from full or 7 before empty. Please refer to the example code for the proper sequence or refer to the Cypress data sheet.

6. Master INT EN is the master interrupt enable. Default is 0. If set to 1 then the RX, TX , PAE, or PAF interrupts can occur based on individual interrupt enables. If the master interrupt enable is off [0] then no interrupts will be generated. The status register can see the interrupt requests to allow polled operation.

7. INT EXT RX CLK is used to select the reference clock to the RX state machine and FIFOs. When ‘0’ the IP clock is used to allow the interface to keep up with the IP Bus requirements. Default is 0. Normal operation is 1.

BIS_CNTL3

[$16 BISERIAL Control Register Port read/write

CONTROL REGISTER 2	
DATA BIT	**DESCRIPTION**
14-13	CLK Source
12	CLK Post Selector
11-0	Divisor

FIGURE 6 IP-BISERIAL-RTN2 CONTROL REGISTER 3 BIT MAP

Clock Pre-Selector

00	IP CLK
01	oscillator
10	external
11	IP CLK

The clock pre-selector is used to select which reference clock to use with the divisor hardware. [The clock source] The external clock is TX_RDY.

Divisor [11-0] are the clock divisor select bits. The clock source is divided by a counter and the select bits pick which clock is used to drive the IO read-back registers. The reference clock for the counter is selected with the CLK Pre-Selector. The output frequency is {reference / [2(n+1)]}. N≥1. The reference oscillator is XXX MHz. in frequency [not installed in RTN2. The counter divides by N+1 due to counting from 0 ->n before rolling over. The output is then divided by 2 to produce a square wave output.

Post Selector when '1' sets clock out to clock divided, when '0' sets clock out to pre-selector reference value. For the “natural” rate select ‘0’.

Please note that the 485 buffers are rated for 10 MHz. With most systems the larger divisors will be used. The smaller divisors are provided for use with external oscillators and the external clock line.

BIS_Vector

[$06] BISERIAL Interrupt Vector Port
The Interrupt vector for the BISERIAL is stored in this byte wide register. This read/write register is initialized to 'xxFF' upon power-on reset or software reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered. The interrupt is automatically cleared when the CPU acknowledges the interrupt.

BIS_STAT0

[$08] BISERIAL Status Port [read only]

Data Bit	Status	
11	User Input	
10	'0'	
9	RX_STB	
8	TX_STB	
7	FTX_FF	1 = transmit FIFO full
6	FTX_PAE	1 = transmit FIFO almost empty
5	FTX_MT_1	1 = transmit FIFO 1 empty
4	FTX_MT_0	1 = transmit FIFO 0 empty
3	FRX_FF_0	1 = receive FIFO 0 full
2	FRX_FF_1	1 = receive FIFO 1 full
1	FRX_PAF	1 = receive FIFO almost full
0	FRX_MT	1 = receive FIFO empty

FIGURE 7 IP-BISERIAL-RTN2 STATUS REG 0 BIT MAP

8,9. RX_STB & TX_STB are indicators that a data transfer is in progress.

7-0. The FIFO flags are active high. When the empty bit is '1' then the FIFO is empty. When the empty flag is '0' then the FIFO has at least one piece of data stored. When the Full Flag is set the FIFO is full. When not set then the FIFO still has room.

11 User input data bit. Data is latched with a "D" flip-flop referenced to the IP clock. Data bit is read in from RX CLK.

BIS_STAT1

[$0A] BISERIAL Status Port [read only]

Data Bit	Status	
7	int rqst	1 = interrupt pending
6	Over Run Error	1 = error detected
5	Frame Error	1 = error detected
4	Parity Error	1 = error detected
3	FAF_INT	1 = interrupt pending
2	FAE_INT	1 = interrupt pending
1	RX_INT	1 = Interrupt pending
0	TX_INT	1 = Interrupt pending

FIGURE 8 IP-BISERIAL-RTN2 STATUS REG 1 BIT MAP

1. RX_INT, TX_INT, PAF_INT, PAE_INT are set when the respective interrupt conditions exist and the interrupts are enabled. The master interrupt can be disabled and still have the benefit of the status. The status is cleared when read.

2. Parity, Frame, and Over Run errors are tested for when a reception is in progress. If detected then the status bit is set and the reception continues. The word count shows the number of words . Cleared on read of STAT1.

BIS_STAT2

[$0C] BISERIAL Status Port [read only]

Data Bit	Status
15	MC_ERR 1 = new count written before old count read 0 = no error
12 - 0	CNT12-0 word count

FIGURE 9 IP-BISERIAL-RTN2 STATUS REG 2 BIT MAP

15 MC ERROR is set when a new word count is loaded before status register 2 is read. Old count over-written by new.

12-0. Word count. The word count is updated for each word loaded into the FIFOs. Read the word count to determine the number of words to read. Cleared on read of STAT2. The counter is cleared when the new reception starts. The latch storing the count is loaded when the reception is completed. The counter is updated once per word received. The software has until the next message has been completed before the current count is over-written. The length of time is set by system constraints.

BIS_FTX_W

[$10] BISERIAL TX FIFO write
By writing a to this address data is loaded into the TX FIFO. In addition a write to the Memory Space [any address] will also write to the TX FIFO. The memory space write is a useful feature for software that would naturally auto-increment the address, or systems where the addresses are auto-incremented. For example the PCI3IP carrier card supports 32 bit transfers by writing the lower 16 bits then incrementing the address and writing the upper 16 bits. A 32 bit transfer can be made on the PCI bus saving system bandwidth.

BIS_FTX_R

[$22] BISERIAL TX FIFO read
A loopback path is provided for the TX FIFOs to allow the host to read the data stored in the TX FIFOs. Reading from this address fetches data from the TX FIFOs. The clock must be set to IP for source and '0' for the postselector before reading from this register. *Once the data is read from the FIFO the data is no longer available for transmission*.

BIS_FRX_W

[$20] BISERIAL RX FIFO write

A loopback path is provided for the RX FIFOs to allow the host to load data into the RX FIFOs. Writing to this address loads data into the RX FIFO. This operation competes with and should not be performed during normal operation. The clock selector needs to be set to internal for the RX reference clock. CNTL2.

BIS_FRX_R

[$40] BISERIAL RX FIFO Read
The data stored into the receive can be accessed through this port. A read from the Memory space [any address] will also access this port. Use the memory space for 32 bit auto-incrementing accesses and faster transfers if your carrier supports that. Non-compelled DMA is also an option with the MEM space access.

PAE PAF Programming

To use the PAF and PAE flags with a setting other than the default of 7 programming. The FIFOs are configured as two 8 bit data paths in parallel The upper byte is where the flags are generated [D15-8]. The lower byte flags are not used. The data path carries the programming information when the FIFO is taken out of reset with the LD controls set low. The RX FIFO is written with the loop-back path and requires the clock settings for loop-back. The RX and TX FIFO can be programmed using the following procedure.

- reset the FIFOs and place into the two enable mode
- program the PAE/PAF flag to trigger at new value
- put into operational mode

- set LD control low with enable hi – set low for flag to be programmed or both
- set LD control low with enable low
- set LD control low with enable hi to clear the FIFO with the WE control in the dual mode

- program the PAE to be at the new value
- first write with LD low = LSB of PAE, second = upper bits of PAE
  third = LSB of PAF and 4th = upper bits of PAF */
- raise LD Control hi to resume normal FIFO operation

Interrupts

All IP Module interrupts are vectored. The vector from the IP-BISERIAL-RTN2 comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-BISERIAL-RTN2 state machines generate an interrupt request when a transmission or reception is complete and the INTEN bits in the control registers are set. The transmission is considered complete when the strobe line is deactivated. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector and clear the request when accessed by the CPU. The source of the interrupt is obtained by reading BIS_STAT1. The status remains valid until the status register is read. The interrupt status is auto-cleared when the status register is accessed. Some carrier boards prefetch data. If your carrier board prefetches the interrupt status then the status may be cleared when the SW goes to look at it. If this is an issue then reading the BIS_STAT1 before BIS_STAT0 is usually a solution.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BIS_CNTL2 register. The individual enables for TX and RX are controllable through BIS_CNTL0 and BIS_CNTL1. The enable operates before the interrupt holding latch which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to reset the board, service the request, or disable the interrupt. Toggling the interrupt enable low will clear the interrupt, the interrupt enable can be set back to enabled immediately. TX_INT_EN enables and clears the TX interrupt and RX_INT_EN enables and clears the RX interrupt request.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled and the Rx or TX or both enabled. When BIS_STAT1 shows and interrupt pending the appropriate FIFO action can take place and the enable toggled to remove the interrupt request then one extra read of the BIS_STAT1 to make sure that the interrupt request is cleared before starting the next transfer. Reading the BIS_STAT1 register does clear the interrupt status, but if the source of the status is still pending [interrupt request] then the status can become set again before the SW has a chance to clear it out. Hence the necessity of

one extra read for clearing purposes.

Power on initialization will provide a cleared interrupt request, interrupts disabled, and interrupt vector of $FF.

The programmable interrupts operate in much the same way. The programmable interrupts are triggered by FIFO level instead of TX / RX completion. The interrupts are cleared with the individual enables or the INTACK cycle. The levels are programmable to allow the software to respond before the FIFO is empty or full so that longer transfers can be handled without using larger FIFOs.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IPs I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically.

Standard data in the ID PROM on the IP-BISERIAL-RTN2 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-BiSerial-IO board will be recorded with a new code in the DRIVER ID location. -RTN2 is set to '2' with a customer number of 0x10.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($01)
0D	Revision	($A0)
0F	reserved	($10)
11	Driver ID, low byte	($02)
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($b9)

FIGURE 10 IP-BISERIAL-RTN2 ID PROM

Loop-back

The Engineering kit has reference software which includes an external loop-back test. The test requires and external cable with the following pins connected.

Data+ 8 - 20
Data- 9 - 21
Strobe+ 14 - 26
Strobe- 15 - 27
User out/in+ 17 - 23
User out/in- 18 – 24

In addition the reference clock needs to be connected to a differential clock source. We used the IP-Debug-IO II card with the built in locations for an oscillator and differential driver to create the clock.

TX_RDY+ 5
TX_RDY- 6

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-BISERIAL-RTN2. Pins marked n/c below are defined by the specification, but not used on the IP-BISERIAL-RTN2. Also see the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		n/c		5		30	
	D2		MEMSEL*		6		31
D3		n/c		7		32	
	D4		IntSel*		8		33
D5		n/c		9		34	
	D6		IOSel*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		IntReq0*			17		42
	D14		A4		18		43
D15		n/c		19		44	
	BS0*		A5		20		45
BS1*		n/c		21		46	
	n/c		n/c		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		GND		25		50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 11 IP-BISERIAL-RTN2 LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-BISERIAL-RTN2. Also see the User Manual for your carrier board for more information.

GND	RXSTB+	1	26		
REFCLK_422+	RXSTB-	2	27		
REFCLK_422-	GND	3	28		
GND	RX_RDY_TTL	4	29		
TXRDY+	GND	5	30		
TXRDY-	RX_DATA_TTL	6	31		
GND	GND	7	32		
TXDATA +	RX_CLK_TTL	8	33		
TXDATA -	GND	9	34		
GND	RX_STB_TTL	10	35		
TXCLK +	GND	11	36		
TXCLK -	TX_RDY_TTL	12	37		
GND	GND	13	38		
TXSTB +	GND	14	39		
TXSTB -	R_C_TTL_IN	15	40		
GND	GND	16	41		
RX_RDY_422+	GND	17	42		
RX_RDY_422-	TX_DTA_TTL	18	43		
GND	GND	19	44		
RXDATA +	GND	20	45		
RXDATA -	TX_CLK_TTL	21	46		
GND	GND	22	47		
RXCLK +	GND	23	48		
RXCLK -	TX_STB_TTL	24	49		
GND	GND	25	50		

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 12 IP-BISERIAL-RTN2 IO INTERFACE

RTN2 uses the 422 versions of data, clock and strobe. The external clock reference is received on TXRDY for this revision. TX refers to the transmit and RX refers to Receive relative to the BiSerial board. User out on RXRDY and user in on RXCLK pins.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the IP-BISERIAL-RTN2 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-BISERIAL-RTN2 does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within .7 volts of ground potential.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-BISERIAL-RTN2 is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BISERIAL design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package.

Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
InterNet Address support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Serial Interface:	RS-485 RDY, Data, CLK, STB RX and TX
TX CLK rates generated:	IP CLK, Oscillator, User CLK input plus 12 bit divider to create output frequencies
Software Interface:	Control Register, ID PROM, Vector Register, Status Port, FIFO
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	Word in IO Space (see memory map) Word in ID Space Word or LW in Memory space Vectored interrupt
Access Time:	back-to-back cycles in 500ns (8Mhz.) or 125 nS (32 Mhz.) to/from FIFO
Wait States:	1 to ID space, 2 to IO, MEM or INT space except for loop-back FIFO access
Interrupt:	Tx interrupt at end of transmission Rx interrupt at end of transmission Programmable Almost Empty Programmable Almost Full
DMA:	No Logic Interface DMA Support implemented at this time Memory space non-compelled supported to FIFOs.
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{0}C for uniform heat across IP
Power:	Max. **220** mA @ 5V

Order Information

IP-BISERIAL-RTN2	IP Module with 1 Tx and 1 Rx serial channel, Programmable data rates RTN2 protocol support, RS-485 drivers and receivers 16 bit IP interface
Tools for IP-BISERIAL-RTN2	IP-Debug-Bus - IP Bus interface extender http://www.dyneng.com/ipdbgbus.html IP–Debug-IO - IO connector breakout http://www.dyneng.com/ipdbgio.html
Eng Kit–PMC-BISERIAL	IP-Debug-IO - IO connector breakout IP-Debug-Bus IP Bus interface extender Technical Documentation, 1. PMC-BISERIAL Schematic 2. PMC-BISERIAL Reference test software Data sheet reprints are available from the manufacturer's web site reference software.