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User Manual

IP-BiSerial-HDP

Bi-directional Serial Data Interface IP Module

Revision C
Corresponding Hardware: Revision A
PROM Revision C

IP-BiSerial-HDP
Bi-directional Serial Data Interface
IP Module

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Product Description

IP-BISERIAL is part of the IP Module family of modular I/O components. The IP-BISERIAL is capable of providing multiple serial protocols. The standard protocol implemented provides a Data, Clock and Strobe interface with Ready control. The –HDP version is a custom modification. The main modifications include lsb first format, gated clock, and custom strobe timing.

In addition to the HDP version other custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there we can redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please contact Dynamic Engineering with your custom application.

The IP-BISERIAL-HDP supports both 8 and 32 MHz IP Bus operation. The IP Clock is used to derive the reference clock for the serial operation. Please be sure to set the appropriate clock selection after reset to insure proper operation. Please refer to the programming section for details.

Both single ended and differential I/O are available on the serial signals. The differential drivers and receivers conform to the RS-485 specification (exceeds RS-422). The RS-485 input signals are terminated with 180Ω. The single ended driver signals are characterized as open drain drivers with 24 mA of sink. For convenience a 2KΩ pull-up is supplied on board, for faster termination a second pull-up can be added at the receiving end of the circuit. Single ended signals are received through 33Ω resistors. Care should be taken with the single ended signals, as transients can damage the board.

All configuration registers support read and write operations for maximum software convenience. Word and byte operations are supported (please refer to the memory map).

The IP-BISERIAL-HDP conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Since the IP maintains plug and software compatibility while mounted on different form factors, system prototyping may be done on one IP Carrier board, with final system implementation done on a different one.

The serial channels are supported by 1K by 16 bit FIFOs, which support word accesses. On-board read/write paths exist for FIFO loop-back testing.

The serial transmit channel reads data from the output FIFO and sends it out serially, lsb first, 16 bits plus parity. The data strobe frames each 17-bit word and 17 data clocks define the bit periods. When the FIFO becomes empty the transmission completes, which can be configured to cause a transmit interrupt.

In the interrogate / test mode the IP-BISERIAL-HDP also receives data. While the data strobe is low, 17 clocks are output to clock in the receive data word. If the parity bit indicates the word was correct, a receive interrupt is generated, otherwise, the parity error status bit is set. An interrupt can also be generated when the input FIFO becomes almost full as defined by the programmable almost full FIFO level. The message can be read directly from the input FIFO.

The IP-BISERIAL-HDP operates with a 100 kHz data clock that is derived from the IP clock. A selectable divider allows proper operation with either an 8 or 32 MHz IP clock. Please refer to the clock selection in the programming section for details.

Interrupts are supported by the IP-BISERIAL-HDP. An interrupt occurs at the end of the transmission when data is sent or when a valid data word is received. The programmable interrupts are also available to provide an almost empty indicator for Tx and almost full indicator for Rx. The interrupts are individually maskable and the interrupt vector is user programmable by a read / write register. The interrupt occurs on IntReq0. The level status is also available for the FIFOs making it possible to operate in a polled mode.

Theory of Operation

The IP-BISERIAL-HDP is designed for the purpose of transferring data from one point to another with a serial protocol.

The IP-BISERIAL-HDP features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BISERIAL design. Only the drivers, receivers, boot PROM and FIFOs are external to the Xilinx device.

The IP-BISERIAL-HDP is a part of the IP Module family of modular I/O products. It meets the IP Module Vita Standard. In standard configuration it is a Type 1 mechanical with no components on the back of the board and one slot wide. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

A logic block within the Xilinx device contains the decoding and timing elements required for the host CPU to interface with the IP bus. The timing is referenced to the 8 or 32 MHz IP logic clock. The IP responds to the ID, INT, MEM, and IO selects. The DMA control lines are connected to the Xilinx for future revisions, but are not used at this time. The BISERIAL design requires wait states for read or write cycles to any address. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host removes the SEL line. Local timing terminates a write cycle prior to the SEL being deasserted. If no hold cycles are requested by the host, the IP-BISERIAL-HDP is capable of supporting 16+ MB per second data transfer rate with a 32 MHz reference rate.

The serial I/O can support many protocols. The HDP status mode timing for a 17-bit transfer is shown in figure 1. The clock is gated, the data changes on the rising edge and is valid on the falling edge of the clock, and the active high strobe frames each word.

The serial transmit channel reads data from the output FIFO and sends it out serially, lsb first, 16 bits plus parity. The data strobe goes high five microseconds before the rising edge of the first data clock. There is a 5 uS delay from the falling edge of the last clock before the Strobe goes low, followed by a 5 uS delay while the Strobe is low, followed by a 5 uS delay before the next rising edge of the clock. If a delay has been programmed the additional time is added on during the strobe low time. The added time is in 10 uS increments.

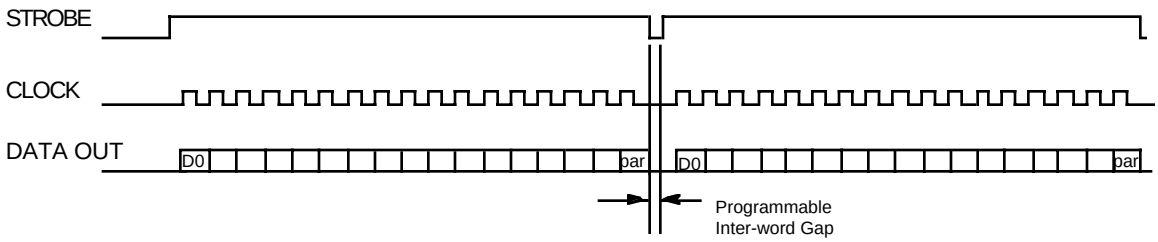

FIGURE 1 IP-BISERIAL-HDP STATUS MODE TIMING

The interrogate / test mode timing is shown in figure 2. In this mode The transmission is followed by data read back from the target. There is a 5 uS delay from the rising edge of the strobe to the first rising edge of the clock. At the end of the transmission portion there is a 5 uS delay from the falling edge of the last clock before the Strobe goes low. There is a 15 uS delay before the next rising edge of the clock. If a delay has been programmed the additional time is added on during the strobe low time before the first clock. The added time is in 10 uS increments. When the Transmit FIFO is empty the process stops after the read.

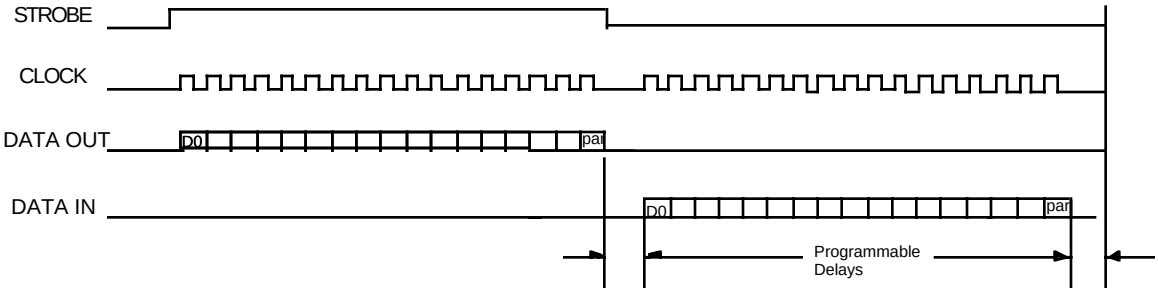

FIGURE 2 IP-BISERIAL-HDP INTERROGATE / TEST MODE TIMING

A pair of state machines within the FPGA control all transfers between the FIFO and FPGA, and the FPGA and the data buffers. The TX state machine reads from the transmit FIFO and loads the shift register before sending the data. The Rx state machine receives data from the data buffers and takes care of moving data from the shift register into the Rx FIFO.

Data transmission can be initiated after the output FIFO is loaded. When the start bit is detected high, the transfer begins. The data is read from the FIFO and loaded into the shift register. The strobe is asserted high, and five microseconds later the LSB is present at the output of the data buffer and the first data clock is asserted. One-half clock period later the Falling

edge of the data clock is driven to the output clock buffer. One-half clock period later the data is transitioned to the next value. The LSB+1 is now on the data lines. The process repeats until the first word and parity bit are transferred, at which time the strobe is de-asserted for five microseconds. Assuming that there is more data to be sent in the FIFO, a second word is read and loaded into the shift register and sent out onto the bus. The process is repeated until the FIFO is detected to be empty when it is time to load. The data stream is continuous.

If the interrogate / test mode is selected, the data transmissions are alternated with data receptions. This occurs during the low period of the data strobe. Five microseconds after the strobe goes low, 17 data clocks are output to shift in the receive data. The data should change on the rising edge of this clock and is latched on the falling edge. Five microseconds after the falling edge of the last receive clock, the strobe goes high for another transmit cycle.

Data is loaded into the receive shift register on the falling edge of the data clock. Once a word has been received the data is loaded into the receive FIFO. If the parity bit is correct, an interrupt to the host is generated (if enabled) otherwise the parity error bit is set. The receiver also checks for over-run errors, and if detected sets the appropriate bit in STAT1.

Address Map

Function		Offset	Width	Type
BIS_CNTL0	EQU	$00	byte on word boundary	read / write
BIS_CNTL1	EQU	$02	byte on word boundary	read / write
BIS_CNTL2	EQU	$04	byte on word boundary	read / write
BIS_VECTOR	EQU	$06	byte on word boundary	read / write
BIS_STAT0	EQU	$08	word	read
BIS_STAT1	EQU	$0A	word	read / write
time_delay	EQU	$0E	byte on word boundary	read / write
BIS_FTX_W	EQU	$10	word	write
BIS_FTX_R	EQU	$22	word	read
BIS_FRX_W	EQU	$20	word	write
BIS_FRX_R	EQU	$40	word	read

FIGURE 3 IP-BISERIAL-HDP INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-BISERIAL-HDP. The addresses are all offsets from the IO space base address. The BIS_FTX_W and BIS_FRX_R ports are also mapped to the entire MEM address space and the BISERIAL_IDPROM is mapped to the ID space. These addresses are supplied by the carrier board in which the IP is installed.

Programming

Programming the IP-BISERIAL-HDP requires only the ability to read and write data in the host's I/O space. The IP Carrier board determines the base address of this address space. This documentation refers to the base address as the beginning of the I/O space for the slot in which the IP is installed.

In order to transmit data the software is only required to load data into the FIFOs and enable the Tx state machine. If desired, the interrupt can be enabled and the interrupt vector written to the vector register. If the interrogate/test mode is selected data will be loaded into the FIFOs as it is received. The parity is checked for each word received and an error bit is set if detected. Odd parity is the default, but even parity or no parity can be selected if desired.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example $40 is a valid user vector for the Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the desired interrupts enabled. Interrupts can be generated when the transmission completes, when a valid word is received, when the transmit FIFO becomes almost empty, or when the receive FIFO becomes almost full.

The end of transmission interrupt will indicate to the software that an outgoing message has been started and that the message has terminated. If both the Tx and Rx interrupts are enabled then the SW needs to read BIS_STAT1 to see which source caused the interrupt. In order to avoid missing an interrupt, the bits in this register must be explicitly cleared by writing the appropriate bit as a '1'. It is a good idea to clear the status bits before a transfer is enabled to insure that the RX_INT or TX_INT value read by the interrupt service routine came from the current reception.

The IP-32 clock-rate bit should be set when operating with a 32 MHz IP clock in order to properly generate the 100 MHz data-clock.

Messages longer than 2K bytes can be accommodated by special ordering HW with larger FIFOs or by using the MT and Full flags on the FIFOs to poll during the transfer…fill the Tx FIFO and when not full add more data until full. On the receive side poll and when not empty read the data until empty. The PAE flag is to provide a length programmable almost empty interrupt to allow the Tx side to operate in an interrupt driven mode with longer

messages. Similarly the PAF can be used to provide an almost full interrupt to the receive side host to allow interrupt driven long message capability.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

REGISTER DEFINITIONS

BIS_CNTL0

$00 BISERIAL Control Register Port read / write

CONTROL REGISTER 0	
DATA BIT	**DESCRIPTION**
7	PARITY EVEN
6	PARITY DISABLE
5	INT ENABLE FAE
4	INT ENABLE TX
3	spare
2	RX LOOP-BACK DATA ENABLE
1	START INTERROGATE / TEST MODE
0	START STATUS MODE

FIGURE 4 IP-BISERIAL-HDP CONTROL REGISTER 0 BIT MAP

0. START STATUS MODE is set to send data. The bit is auto cleared at the end of a transmission.

1. START INTERROGATE / TEST MODE is set to send and receive data. The bit is auto cleared at the end of a transmission.

2. RX LOOP-BACK DATA ENABLE is set to send data on both the high and low data strobe periods when in interrogate / test mode. This is used solely for testing and should not be set in normal operation.

4. INT ENABLE TX is the Interrupt Enable bit for the Transmit channel. The default state is off. If set to '1', and the master interrupt enable is also set, then an interrupt is generated when the transmission is complete.

5. INT ENABLE FAE is the Interrupt Enable bit for the Programmable Almost Empty condition. The default state is off. If set to '1', and the master interrupt enable is also set, then an interrupt is generated when the FIFO level falls to the almost empty count.

6. PARITY DISABLED when set to '1' causes the parity bit to always be zero. The default is '0' or parity enabled.

7. PARITY EVEN when set to '1' causes even parity to be used to calculate the parity bit. The default is '0' or odd parity.

BIS_CNTL1

$02 BISERIAL Control Register Port read / write

CONTROL REGISTER 1	
DATA BIT	**DESCRIPTION**
8	RX STROBE POLARITY
7	PARITY DISABLE
6	PARITY EVEN
5	INT ENABLE FAF
4	INT ENABLE RX
3	spare
2	spare
1	EXT / INT RX STROBE
0	RX_TTL_422

FIGURE 5 IP-BISERIAL-HDP CONTROL REGISTER 1 BIT MAP

0. RX_TTL_422 is the control bit to select whether the data, clock, and strobe should be received as TTL or 422 signals. Default state = '0' = 422 [485], a '1' selects TTL inputs.

1. EXT / INT RX STROBE is used to select the source of the data strobe to the Rx state machine and FIFOs. When '1' the external strobe is used for loop-back testing only. When '0' the internal strobe is used. The default is '0', which is the normal operational state.

4. INT ENABLE RX is used to enable the receive interrupt. The default is disabled. If set to '1', and the master interrupt enable is also set, then an interrupt is generated when a valid data word is received.

5. INT ENABLE FAF is used to enable the Programmable Almost Full interrupt. The default is disabled. If set to '1', and the master interrupt enable is also set, then an interrupt is generated when the receive FIFO fills to the almost full condition.

6. PARITY DISABLED when set to '1' causes the parity bit to be ignored. The default is '0' or parity enabled.

7. PARITY EVEN when set to '1' causes even parity to be used to calculate parity. The default is '0' or odd parity.

8. RX STROBE POLARITY when set to ‘1’ causes data to be received and stored when the data strobe is high. This mode is used for test only. The default and normal operational state is ‘0’: receive data when the strobe is low.

BIS_CNTL2

$04 BISERIAL Control Register Port read/write

CONTROL REGISTER 2

DATA BIT	DESCRIPTION
8	HDP_GO_NOGO Enable
7	MASTER INT ENABLE
6	FORCE INTERRUPT
5	FIFO IP CLOCK
4	FIFO ENABLE
3	FRX_LD
2	FTX_LD
1	IP-32 CLOCK-RATE
0	HDP_GO_NOGO_LED

FIGURE 6 IP-BISERIAL-HDP CONTROL REGISTER 2 BIT MAP

0. HDP_GO_NOGO is a status bit to communicate with external equipment. This bit drives both the RX_RDY_422 and RX_RDY_TTL output pins. The RX_RDY_TTL is used to connect to an LED. The LED does not have a power source. When high the pull-up associated with the HDP_GO_NOGO_LED signal sources the LED. When low the LED is turned off and the current sunk by the 125.

1. IP-32 CLOCK-RATE is set to ‘1’ when using a 32 MHz IP clock. The default is ‘0’ (8 MHz IP clock). This bit selects the divisor used to generate the 100 kHz data clock.

2,3. FRX_LD is tied to the RX FIFO WE2/_LD pin. FTX_LD is tied to the Tx FIFO WE2/_LD pin. When the FIFOs are taken out of reset it is possible to set-up the FIFO to accept commands to program the levels at which the programmable almost empty and programmable almost full signals operate. ***In the standard transfer mode these pins are set high before FIFO ENABLE is asserted to use as a second WE control pin***. If the PAE and PAF flags are to be used at a different than default depth then the flags will require programming. The defaults are 7 from full and 7 before empty. Please refer to the PAE PAF Programming section or the Cypress data sheet for the proper sequence.

4. FIFO ENABLE is used to reset the FIFOs. The default state is ‘0’ or disabled. The FIFOs must be enabled to be used to store data. This signal must be set high then low then high while the FIFO clock is running to cause a proper reset with guaranteed flag operation. We suggest using the IP clock as the reference for this process. Please refer to FIFO IP CLOCK below and FTX_LD and FRX_LD above.

5. FIFO IP CLOCK when ‘1’ selects the IP clock for the Tx FIFO read and Rx FIFO write clocks (the IP clock is always used for the Tx FIFO write and Rx FIFO read clocks). This is used for FIFO loop-back testing and when resetting the FIFOs to guarantee a proper reset operation. The default is ‘0’, which is the normal operational setting.

6. FORCE INTERRUPT is used to create an interrupt for test and software development purposes. Set the bit to ‘1’ to cause the interrupt and clear the bit to remove the interrupt. This requires that the master interrupt enable is set to ‘1’ to have an effect.

7. MASTER INT ENABLE is the master interrupt enable. Default is 0. If set to 1 then the RX, TX, PAE, or PAF interrupts can occur based on individual interrupt enables. If the master interrupt enable is off (‘0’) then no interrupts will be generated. The status register can still see the interrupt requests to allow polled operation.

8. The HDP_GO_NOGO Enable has two functions. Initially during power on reset the FPGA defaults to tri-state on the control line to the ‘125 and direction on the 485 transceiver associated with the GO_NOGO signal. External resistors set the direction to input on the transceiver and enabled on the 125. The 485 signal pair is set to ‘0’ with a pull-down on the ‘+’ side and a pull-up on the ‘-‘ side. The ‘125 has a grounded input; the output is driven low due to the pull-down on the enable signal. After power-on initialization is over the default condition from the FPGA is consistent with the resistor controlled reset state. Later when the software is ready to begin communication the enable can be set; the direction of the transceiver changes to output and the control line to the ‘125 is taken out of reset allowing the definition of the GO_NOGO bit to control the 125. See the Bit 0 definition.

BIS_VECTOR

$06 BISERIAL Interrupt Vector Port read / write
The interrupt vector for the BISERIAL is stored in this byte wide register. This read / write register is initialized to 0XFF upon power-on reset or software reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered.

BIS_STAT0

$08 BISERIAL Status Port [read only]

Data Bit	Status	
9	OVERTEMP	External input
8	ENABLE	External input
7	FTX_FF	1 = transmit FIFO full
6	FTX_PAE	1 = transmit FIFO almost empty
5	FTX_MT_1	1 = transmit FIFO 1 empty
4	FTX_MT_0	1 = transmit FIFO 0 empty
3	FRX_FF_0	1 = receive FIFO 0 full
2	FRX_FF_1	1 = receive FIFO 1 full
1	FRX_PAF	1 = receive FIFO almost full
0	FRX_MT	1 = receive FIFO empty

FIGURE 7 IP-BISERIAL-HDP STATUS REG 0 BIT MAP

7-0. The FIFO flags are active high. When the empty bit is ‘1’ then the FIFO is empty. When the empty flag is ‘0’ then the FIFO has at least one piece of data stored. When the Full Flag is set, the FIFO is full. When not set then the FIFO still has room.

8. ENABLE is controlled by an external input through the TXRDY+ input pin. A 2kΩ onboard pull-up is connected to this signal to allow for a mechanical switch input.

9. OVERTEMP is also controlled by an external input through the TX_RDY_TTL input pin. This signal is assumed to be driven high as well as low, so no pull-up is provided.

BIS_STAT1

$0A BISERIAL Status Port [read / write]

Data Bit	Status	
8	INT REQUEST	1 = interrupt pending
7	PARITY ERROR	1 = error detected
6	OVERRUN ERROR	1 = error detected
5	spare	
4	spare	
3	FAF_INT	1 = interrupt pending
2	FAE_INT	1 = interrupt pending
1	RX_INT	1 = Interrupt pending
0	TX_INT	1 = Interrupt pending

FIGURE 8 IP-BISERIAL-HDP STATUS REG 1 BIT MAP

0-3. RX_INT, TX_INT, FAF_INT, FAE_INT are set when the respective interrupt conditions exist. The individual interrupt enables and the master interrupt enable must be set to cause a system interrupt.

6. OVERRUN ERROR occurs during a reception when an attempt is made to store a received word when the Rx FIFO is full. This results in a loss of data, which is indicated by this status bit being set to '1'.

7. PARITY ERROR is tested for when a reception is in progress. If detected then this status bit is set to '1' and the reception continues.

8. INT REQUEST is high when an enabled interrupt condition exists. This bit is not masked by the MASTER INT ENABLE.

Note: status bits 0-3,6,7 in this register are individually clearable by writing a '1' to the corresponding bit.

BIS_FTX_W

$10 BISERIAL TX FIFO Write

By writing a to this address data is loaded into the Tx FIFO. In addition a write to the Memory Space (any address) will also write to the Tx FIFO. The memory space write is a useful feature for software that would naturally auto-increment the address, or systems where the addresses are auto-incremented.

BIS_FTX_R

$22 BISERIAL TX FIFO Read

A loop-back path is provided for the Tx FIFO to allow the host to read the data stored in the Tx FIFO. Reading from this address fetches data from the Tx FIFO. The FIFO IP CLOCK bit in BIS_CNTL2 must be set to '1' before reading from this register. *Once the data is read from the FIFO the data is no longer available for transmission*.

BIS_FRX_W

$20 BISERIAL RX FIFO Write

A loop-back path is provided for the Rx FIFO to allow the host to load data into the Rx FIFO. Writing to this address loads data into the Rx FIFO. This operation competes with and should not be performed during normal operation. The FIFO IP CLOCK (BIS_CNTL2 bit5) needs to be set to '1' to select the IP clock for the Rx reference clock.

BIS_FRX_R

$40 BISERIAL RX FIFO Read

The data stored in the receive FIFO can be accessed through this port. A read from the Memory space (any address) will also access this port. Use the memory space for 32 bit auto-incrementing accesses and faster transfers if your carrier supports that. Non-compelled DMA is also an option with the MEM space access.

Time_Delay

$0E BISERIAL Time Delay Definition Register [read / write]

Data Bit	Status	
7-0	time_delay	Count for time between words

FIGURE 9 IP-BISERIAL-HDP TIME DELAY BIT MAP

The Time_Delay register is used in both the transmit and the interrogate modes.

For transmit the Time_Delay specifies the active low time of the strobe. The minimum time is 5 uS. Each count of time_delay adds 10 uS. Gap time = [5+ (time_delay * 10)]uS.

For the interrogate mode the time after the strobe goes low and before the clock starts up again is [10 + (delay_time * 10)]uS. Similarly the time from the falling edge of the last clock before the strobe is driven high is [10 + (delay_time * 10)]uS.

PAE PAF PROGRAMMING

To use the PAF and PAE flags with a setting other than the default of seven, the FIFO must be programmed. The FIFOs are configured as two 8-bit data paths in parallel. The upper byte is where the programmable flags are generated [D15-8]. This data path must carry the programming information when the FIFO is taken out of reset with the LD controls set low. The Rx FIFO is written with the loop-back path and requires the clock settings for loop-back. The Rx and Tx FIFO can be programmed using the following procedure.

1. Reset the FIFOs and place into the programmable flag mode.
2. Program the PAE / PAF flag to trigger at new value.
3. Put into operational mode.

Step 1.
• Set LD control low with enable hi – set low for flag levels to be programmed.
• Keep LD control low with enable low.
• Keep LD control low with enable high to clear the FIFO with the WE control in the load mode.

Step2
• Write the new trigger levels on upper byte [D15-8] to the Tx and Rx FIFO write ports, keeping the LD controls low.
• first write = LSB of PAE, second = upper bits of PAE
third = LSB of PAF and 4th = upper bits of PAF

Note: All writes must be made to both FIFOs in order to load the correct registers even though only the TX almost empty and Rx almost full are connected.

Step 3
• Set LD Controls high to resume normal FIFO operation.

INTERRUPTS

All IP Module interrupts are vectored. The vector from the IP-BISERIAL-HDP comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-BISERIAL-HDP state machines generate an interrupt request when a transmission is complete or a valid data word is received and the enable bits in the control registers are set. The transmission is considered complete when the last word in the FIFO is sent. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector. The source of the interrupt is obtained by reading BIS_STAT1. The status remains valid and the interrupt remains active until the status register bits are explicitly cleared.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BIS_CNTL2 register. The individual enables for Tx and Rx are controllable through BIS_CNTL0 and BIS_CNTL1. The enables operate after the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to reset the board, clear the latched interrupt bit, or disable the interrupt. The STAT1 bits must be cleared before the interrupt is re-enabled or another interrupt will be generated. INT ENABLE TX enables the Tx interrupt and INT ENABLE RX enables the Rx interrupt.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled. When BIS_STAT1 shows an interrupt pending the appropriate FIFO action can take place then BIS_STAT1 is written to clear that interrupt request before starting the next transfer.

Power on initialization will provide a cleared interrupt request, interrupts disabled, and interrupt vector of $FF.

The programmable interrupts operate in much the same way. The programmable interrupts are triggered by FIFO levels instead of Tx / Rx completion. The interrupts are cleared by writing the appropriate bit to BIS_STAT1. The levels are programmable to allow the software to respond

before the FIFO is empty or full so that longer transfers can be handled without using larger FIFOs.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IPs I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically.

Standard data in the ID PROM on the IP-BISERIAL-HDP is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-BiSerial-IO board will be recorded with a new code in the DRIVER ID location. HDP is set to 0x01 with a customer number of 0x05.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($01)
0D	Revision	($C0)
0F	reserved	($05)
11	Driver ID, low byte	($01)
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($70)

FIGURE 10 IP-BISERIAL-HDP ID PROM

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable with the following pins connected.

Data+	8 - 20
Data-	9 - 21
Strobe+	14 - 26
Strobe-	15 - 27
Clock+	11 - 23
Clock-	12 – 24

In addition our test fixture has LEDs for the Go_NOGO and switch inputs.

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-BISERIAL-HDP. Pins marked n/c below are defined by the specification, but not used on the IP-BISERIAL-HDP. Also see the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		n/c		5		30	
	D2		MEMSEL*		6		31
D3		n/c		7		32	
	D4		INTSEL*		8		33
D5		n/c		9		34	
	D6		IOSEL*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		INTREG0*		17		42	
	D14		A4		18		43
D15		n/c		19		44	
	BS0*		A5		20		45
BS1*		n/c		21		46	
	n/c		n/c		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		GND		25		50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 11 IP-BISERIAL-HDP LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-BISERIAL-HDP. Also see the User Manual for your carrier board for more information.

GND	RXSTB+	1	26		
REFCLK_422+	RXSTB-	2	27		
REFCLK_422-	GND	3	28		
GND	HDP_GO_NOGO_LED	4	29		
TXRDY+	GND	5	30		
TXRDY-	RX_DATA_TTL	6	31		
GND	GND	7	32		
TXDATA +	RX_CLK_TTL	8	33		
TXDATA -	GND	9	34		
GND	RX_STB_TTL	10	35		
TXCLK +	GND	11	36		
TXCLK -	TX_RDY_TTL	12	37		
GND	GND	13	38		
TXSTB +	GND	14	39		
TXSTB -	R_C_TTL_IN	15	40		
GND	GND	16	41		
RX_RDY_422+	GND	17	42		
RX_RDY_422-	TX_DTA_TTL	18	43		
GND	GND	19	44		
RXDATA +	GND	20	45		
RXDATA -	TX_CLK_TTL	21	46		
GND	GND	22	47		
RXCLK +	GND	23	48		
RXCLK -	TX_STB_TTL	24	49		
GND	GND	25	50		

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

NOTE 2: TXRDY+ is used for the ENABLE input signal, TX_RDY_TTL is used for the OVERTEMP input signal, and RX_RDY_422 and RX_RDY_TTL are both driven by the HDP_GO_NOGO bit in the BIS_CNTL2 register.

FIGURE 12 IP-BISERIAL-HDP IO INTERFACE

HDP uses the 422 versions of data, clock, and strobe. Tx refers to the transmit and Rx refers to Receive relative to the BiSerial board.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-BISERIAL-HDP does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the devices rated voltages**.**

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-BISERIAL-HDP is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of 0.89 W / ^{o}C for uniform heat dissipation. This is based upon the temperature coefficient of the base FR4 material of 0.31 W / m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BISERIAL design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering’s products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
Internet Address support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Serial Interface:	RS-485 Data out, Data in, Clock out, Strobe out. TTL and RS-422 Go / No Go, TTL Enable in, and Over-temp in.
Tx CLK rates generated:	IP CLK, IP CLK / 80, IP CLK / 320.
Software Interface:	Control Registers, ID PROM, Vector Register, Status Ports, FIFOs
Initialization:	Hardware Reset forces all registers to 0 except the Vector Register which resets to 0XFF.
Access Modes:	Word in IO Space (see memory map) Word in ID Space Word or LW in Memory space Vectored interrupt
Access Time:	back-to-back cycles in 500ns (8MHz.) or 125 nS (32 MHz.) to / from FIFO
Wait States:	1 to ID space, 2 to IO, MEM, or INT space except for loop-back FIFO access
Interrupt:	Tx interrupt at end of transmission Rx interrupt when valid word received Programmable Almost Empty Programmable Almost Full
DMA:	No Logic Interface DMA Support implemented at this time Memory space non-compelled supported to FIFOs.
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W / ^{O}C for uniform heat across IP
Power:	Max. **220** mA @ 5V

Order Information

IP-BISERIAL-HDP	IP Module with 1 Tx and 1 Rx serial channel, HDP protocol support, RS-485 drivers and receivers 16 bit IP interface
Tools for IP-BISERIAL-HDP	IP-Debug-Bus - IP Bus interface extender http://www.dyneng.com/ipdbgbus.html IP--Debug-IO - IO connector breakout http://www.dyneng.com/ipdbgio.html ribbon cable – various lengths http://www.dyneng.com/HDRribn50.html Terminal Block to ribbon cable adapter http://www.dyneng.com/HDRterm50.html
Carriers for IndustryPacks®	PCI3IP – 3 slot 1/2 length PCI carrier http://www.dyneng.com/pci_3_ip.html PCI5IP – 5 slot full size PCI Carrier http://www.dyneng.com/pci5ip.html cPCI2IP – 2 slot Compact PCI carrier http://www.dyneng.com/cpci2ip.html
Eng Kit–IP-BISERIAL	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender Technical Documentation, 1. IP-BISERIAL Schematic 2. IP-BISERIAL Reference test software Data sheet reprints are available from the manufacturer's web site reference software.