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User Manual

ccPMC-HOTLink-AP1

Conduction-Cooled
Single-Channel HOTLink® Interface

Revision C
Corresponding Firmware: Revision B
Corresponding Hardware: 10-2009-0103

ccPMC-HOTLink-AP1
Single-Channel HOTLink®
Interface
Conduction-Cooled PMC Module

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Product Description

The ccPMC-HOTLink is part of the PMC Module family of modular I/O components by Dynamic Engineering. It features the Cypress Semiconductor CY7B923/CY7B933 HOTLink® Transmitter/Receiver pair. See the block diagram below:

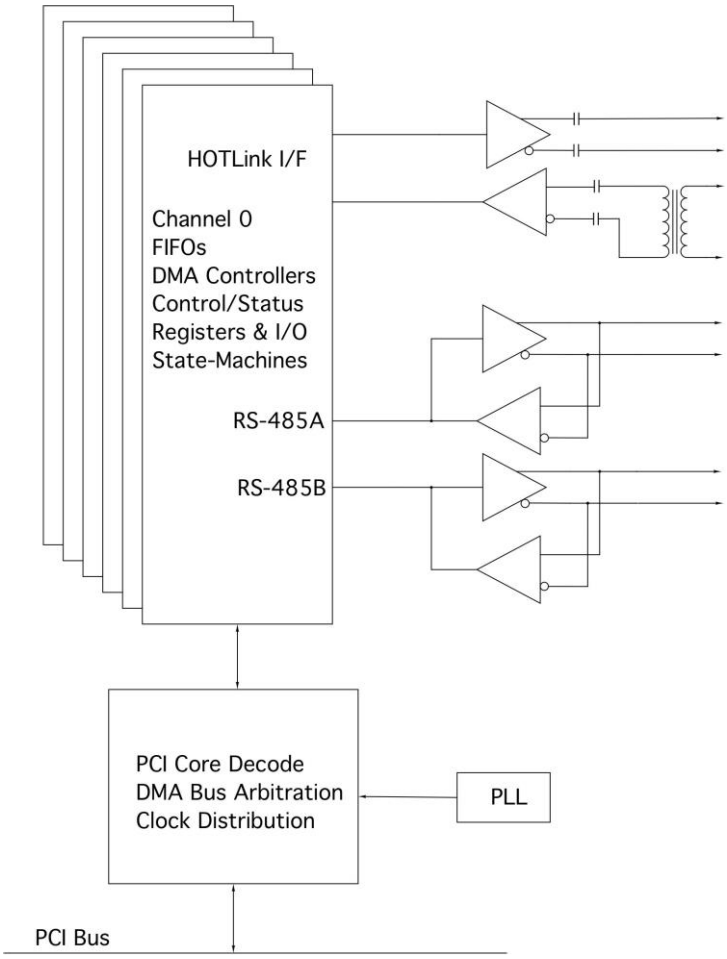


FIGURE 1 PMC-HOTLINK BLOCK DIAGRAM

The HOTLink protocol implemented provides positive emitter-coupled logic (PECL) data inputs and outputs. The transmit byte-rate is determined by the programmed frequency of the PLL A clock output. This clock is multiplied ten times by the HOTLink transmitter which serializes and sends the transmitter byte-wide data-stream which is expanded to 10 bits by the internal 8B/10B encoder.

The PLL is programmed via software over a serial I²C interface. An output and an input 32 by 32-bit FIFOs are used to buffer the data into and out of the PLL. A logic block in the FPGA accesses these FIFOs and generates the waveform timing for the I²C interface. Forty bytes or ten long-words are used to program or read the PLL device.

Six independent HOTLink channels are provided per card, but for this design only a single channel is implemented. The HOTLink channel has four differential I/O signal pairs: A HOTLink differential PECL output, a HOTLink differential PECL input and two bi-directional differential RS-485 lines.

In this design, the HOTLink input is transformer-coupled into a dual 50 Ω termination referenced to 1.8 volts. The signals are then AC-coupled into the HOTLink receiver inputs referenced to 3.5 volt. The HOTLink output is AC-coupled after the bias/termination network and is present in this design for test purposes only.

The HOTLink receiver and transmitter are supported by 64k by 32-bit data FIFOs. These FIFOs can be accessed by single-word accesses as well as DMA burst transfers. The transmit FIFO supports write accesses only and the receive FIFO supports read accesses only, but a FIFO test bit in the channel control register enables the data to be routed from the transmit FIFO to the receive FIFO for a full 32-bit path for loop-back testing of the FIFOs.

The channel also has two bi-directional RS-485 lines running an asynchronous 32-bit msb first protocol with low marking state. The 16x receive clock is supplied by the PLL B clock output. Each line interfaces with a 4k by 32-bit FIFO that supports both write and read single-word accesses. Either line can be configured as a general purpose input or output. Each FIFO can be directly written or read for FIFO testing or normal operation as either a receiver or transmitter.

For both the HOTLink and RS-485 interfaces data is latched and the bus immediately released on a write-cycle. As soon as data is present in the FIFO, the initial word is pre-read to be immediately available for a read cycle. This allows minimal delay on the PCI write to transmit FIFO path and PCI read from the receive FIFO path as well as the accesses for the transmitter and receiver state machines.

The HOTLink board supports various interrupts. An interrupt can be configured to occur when the transmit FIFO is almost empty or the receive FIFO is almost full as well as other events and error conditions. All interrupts are individually maskable and a channel master interrupt enable is provided to disable all interrupts on the channel simultaneously. The current real-time status is always available making it also possible to operate in polled mode.

If and only if an interrupt condition is not enabled for the normal INTA interrupt line, that interrupt condition can be routed to (only one) of the other interrupt lines (INTB, INTC or INTD). The controls for this routing are in the HLNK_BASE_CNTRL control register.

The ccPMC-HOTLink module is conduction-cooled and has no front panel connector. All I/O connections are routed through PN4 and the PMC carrier to the outside world.

The ccPMC-HOTLink conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The ccPMC-HOTLink uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the ccPMC-HOTLink, please let us know. We may be able to do a special build with a different height connector to compensate.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please see our web page for current protocols offered and feel free to contact Dynamic Engineering with your custom application.

Theory of Operation

The HOTLink board features a Xilinx Spartan-6-LX100 FPGA. The FPGA contains the PCI interface, all of the registers, FIFOs and protocol controlling elements of the HOTLink design. Only the transformers, HOTLink and RS-485 transceivers and clock circuitry are external to the Xilinx device.

A logic block within the Xilinx controls the PCI interface to the host CPU. The HOTLink design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather bus-master DMA is provided for in this design. Once the physical address of the first chaining descriptor is written to the DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes represent a long-word indicating the length, in bytes, of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is the direction bit and is set to one if the transfer is from the HOTLink board to host memory, and zero if the transfer is from memory to the board. All descriptor pointers, including the initial descriptor address written to start the DMA, must have the correct direction bit set. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one. This process continues automatically until the last chaining descriptor in the list is processed.

The channel input and output DMA engines interface with the HOTLink transmit and receive FIFOs while the two RS-485 FIFOs are accessed by single-word transfers only.

The channel’s RS-485 lines can be used as general purpose serial inputs or outputs. The entire 32-bit word is read from the FIFO and sent on the line. This RS-485 interface uses a low marking state with a high start-bit. The transmission rate is determined by the PLL clock B, which is divided by 16 to obtain the bit-clock. The receiver uses the 16x clock to recover the bit-stream. The receiver resynchronizes the clock per bit count when transitions are seen in the serial data received.

The ccPMC-HOTLink channel has both a HOTLink receiver and an onboard HOTLink transmitter. The transmitter is present for test purposes only and is connected to the receiver input B by an always-on internal link from transmitter output C. Transmitter output A is AC-coupled to Pn4 for an external loop-back test connection to receiver input A.

There are three storage modes used to write HOTLink data to the receive FIFO. In data-only mode all control characters are stripped from the data-stream and the received HOTLink data (bits 7-0) are written as long-words to the receive FIFO. The first byte received is loaded into byte position zero (bits 7-0), the second byte goes in byte one (bits 15-8) and so on. If the receiver is disabled when a long-word has not been completed, the remaining unfilled bytes are set to zero and the long-word is written to the receiver FIFO.

The other two data storage modes store control characters as well as data. The store-all mode stores all received characters, both data and control. This mode uses 10 bits per character, storing the control/data bit (bit 8) and the symbol violation bit (bit 9). In this mode there are only three bytes per long-word. Byte 0 is stored in bits 9-0, byte 1 is stored in bits 19-10, and byte 2 is stored in bits (29-20). Bits 30 and 31 are not used and are set to zero.

In the compact storage mode the same byte-to-bit mapping is used as the store-all mode, but while all data characters are stored, control characters are only stored if they differ from the character just received. Repeated received control characters are compacted to a single stored control character.

The HOTLink transmitter input data is always stored four bytes to a long-word. The transmitter reads long-words from the transmit FIFO and sends byte zero first followed by byte one, byte two and finally byte three. There are two different transmission modes to select from. One mode sends only data characters as long as the transmitter is enabled and data is present in the transmit FIFO. The other mode replicates the target video-frame as described in figure 2 below.

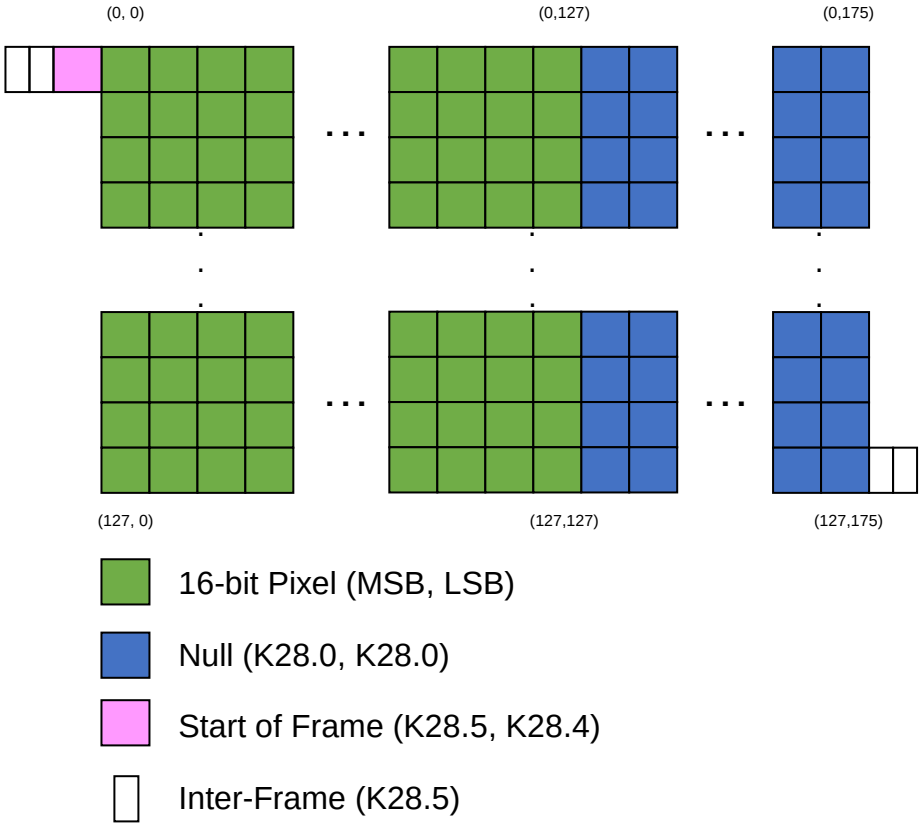


FIGURE 2 PMC-HOTLINK-AP1 VIDEO FRAME

See the description of the channel control register for information on how to select these different modes.

Programming

Programming the ccPMC-HOTLink board requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the board is installed. The VendorId = 0xDCBA. The CardId = 0x0050.

If DMA is to be used it will be necessary to acquire a block of non-paged memory that is accessible from the PCI bus in which to store chaining descriptor list entries. If the Dynamic Engineering device driver is used, the driver will handle all the DMA internal mechanics automatically.

In order to transmit or receive either HOTLink® or RS-485 data, the PLL must be programmed to the desired clock configuration. The PLL is connected to the Xilinx by an I^2C serial bus and its internal registers are loaded with 40 bytes of data that can be derived from a .jed file generated by the CyberClock utility from Cypress semiconductor http://www.dyneng.com/CyberClocks.zip. If you are using our driver, the PLL will be programmed to the default frequency settings when the driver initializes and can be read or re-programmed by an IOCTL call to the base driver.

Routines to use these calls to read and program the PLL are included in the UserApp code provided in the engineering kit for the board. If you are writing your own driver, contact Dynamic Engineering and we can send you a file with code excerpts from our driver and test software that cover each step of the process from parsing the .jed file to controlling the logic that drives the I^2C bus.

Once the relevant enables and configuration options are set, the board will wait to receive HOTLink data and store it in a 64K by 32-bit FIFO. The FIFO almost full level is programmable to whatever level is desired and once that level is reached, an interrupt will be asserted if it has been enabled. The data can then be read from the FIFO using DMA in an efficient manner.

The HOTLink receiver will continue to receive and store characters as long as it is enabled and there remains room in the receive FIFO. When the receiver is disabled, if less than four bytes have been received since the last FIFO write, the last partial word will be written to the FIFO with the unfilled bytes loaded with zeros.

Address Map

Register Name	Offset	Description
HLNK_BASE_CNTRL	0x0000	// Base Control register
HLNK_BASE_USER_INFO	0x0004	// Base User Info read port
HLNK_BASE_INT_STATUS	0x0008	// Base Interrupt Status read port
HLNK_BASE_PLL_FIFO	0x000C	// Base PLL FIFO port
HLNK_CHAN_CNTRL_0	0x0020	// Channel 0 Control register
HLNK_CHAN_STATUS_0	0x0024	// Channel 0 Status register
HLNK_CHAN_FIFO_0	0x0028	// Channel 0 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_0	0x002C	// Channel 0 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_0	0x002C	// Channel 0 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_0	0x0030	// Channel 0 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_0	0x0030	// Channel 0 Receive FIFO data count
HLNK_CHAN_TX_AMT_0	0x0034	// Channel 0 TX almost empty level
HLNK_CHAN_RX_AFL_0	0x0038	// Channel 0 RX almost full level
HLNK_CHAN_485_CNTRL_0	0x003C	// Channel 0 RS-485 Control register
HLNK_CHAN_485_STATUS_0	0x0040	// Channel 0 RS-485 Status register
HLNK_CHAN_485A_FIFO_0	0x0044	// Channel 0 RS-485A FIFO port
HLNK_CHAN_485B_FIFO_0	0x0048	// Channel 0 RS-485B FIFO port
HLNK_CHAN_READ_COUNT_0	0x004C	// Channel 0 Read Count Target

FIGURE 3 PMC-HOTLINK REGISTER OFFSET ADDRESS MAP

Register Definitions

HLNK_BASE_CNTRL

[0x000] Base Control (read/write)

Base Control Register

Data Bit	Description
31-22	Spare
21-20	Received Frame Read Int Select
19-18	Read Count Match Int Select
17-16	Receive FIFO Not Almost Full Int Select
15-14	Transmit FIFO Not Almost Empty Int Select
13-12	Receive FIFO Overflow Int Select
11-10	Receive FIFO Almost Full Int Select
9-8	Transmit FIFO Almost Empty Int Select
7-5	Spare
4	PLL Use Alternate ID
3	PLL Check ID
2	PLL Read Enable
1	PLL Reset
0	PLL Enable

FIGURE 4 PMC-HOTLINK BASE CONTROL REGISTER

All bits are active high and are reset on system power-up or reset, except PLL enable, which defaults to enabled (high) on power-up or reset.

PLL Enable: When this bit is set to a one, the PLL programmer module, used to program and read the PLL, is enabled. When this bit is zero, the PLL programmer is disabled.

PLL Reset: When this bit is set to a one, the PLL programmer will stop processing, if not stopped already, and return to its initial state. When this bit is zero, the PLL programmer is ready to accept control inputs.

PLL Read Enable: When this bit is set to a one and the PLL programmer is enabled, the programmer will perform a read of the PLL device internal registers. The 40 bytes of data obtained will be written into the PLL read FIFO as ten long-words. When this bit is zero and the PLL programmer is enabled, the programmer will write data into the PLL device or simply check for a response to the selected ID value depending on the PLL Check ID control bit.

PLL Check ID: When this bit is set to a one and the PLL programmer is enabled, the programmer will begin a write operation, but will stop after the device ID has been sent. If the ID was acknowledged successfully, the done status will be set and the error status will be cleared. If the ID was not acknowledged successfully, the done status will be cleared and the error status will be set. When this bit is zero and the PLL programmer is enabled, the PLL programmer will perform a write or read operation depending on the PLL Read Enable control bit.

PLL Use Alternate ID: When this bit is set to a one, the device ID sent will be the alternate ID: 0x6A. When this bit is zero, the normal ID: 0x69 will be sent to the PLL device.

Int Selects: These seven two-bit fields control routing interrupts that were not assigned to the normal INTA interrupt line to the INTB, INTC or INTD interrupt lines. The decoding of each two-bit field is as follows:

"00" Interrupt condition is not routed to an interrupt line.
"01" Interrupt condition is routed to INTB.
"10" Interrupt condition is routed to INTC.
"11" Interrupt condition is routed to INTD.

Multiple interrupt conditions can be routed to the same interrupt line. The latched interrupt status for individual interrupt conditions is read from the channel status register and must be cleared by writing a one back to that respective status bit.

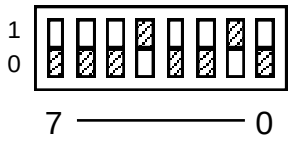
HLNK_BASE_USER_INFO

[0x004] Base User Info – (read only)

User Info Port	
Data Bit	**Description**
31-24	FPGA Design Revision
23-16	FPGA Design ID
15-8	PCI Core Revision
7-0	User ID Switch

FIGURE 5 PMC-HOTLINK BASE STATUS PORT

User ID Switch: The user switch is read through this port. The bits are read as the lowest byte. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



PCI Core Revision: This is the revision that was entered when the core was created, and is the value that is reported to the operating system. Currently this value is 0x00.

FPGA Design ID: This value distinguishes this design from other HOTLink designs using the same PCI vendor/device ID. For this design the value is 0x02.

FPGA Design Revision: The value of the fourth byte of this port is the revision number of the Xilinx design (currently 0x02 – rev B).

HLNK_BASE_INT_STATUS

[0x008] Base Interrupt Status – (read only)

Base Interrupt Status Register

Data Bit	Description
31-19	Spare
18	PLL Error
17	PLL Done
16	PLL Ready
15	Spare
14	PLL Read FIFO Data Valid
13	PLL Read FIFO Full
12	PLL Read FIFO Empty
11	Spare
10	PLL Write FIFO Data Valid
9	PLL Write FIFO Full
8	PLL Write FIFO Empty
7-4	Spare
3	Interrupt Line D Active
2	Interrupt Line C Active
1	Interrupt Line B Active
0	Interrupt Line A Active

FIGURE 6 PMC-HOTLINK BASE STATUS PORT

Interrupt Line A-D Active: These four bits are used to report which interrupt lines are currently active. When a one is read, it indicates that the channel has requested an interrupt on that line; when all four bits are read as zero, no channel interrupt is active.

PLL Write/Read FIFO Empty: When a one is read, it indicates that the corresponding FIFO contains no data; when a zero is read, there is at least one word in the FIFO. Although the FIFO is empty, there may still be one valid data word in the pipeline. The FIFO data valid bit indicates whether this is the case.

PLL Write/Read FIFO Full: When a one is read, it indicates that the corresponding FIFO is full; when a zero is read, there is room for at least one word in the FIFO.

PLL Write/Read FIFO Data Valid: When a one is read, there is valid data available; when a zero is read, there is no valid data available.

PLL Ready: When a one is read, the PLL programmer is idle and ready to accept a new command; when a zero is read, the programmer is actively sending data or reading data to/from the PLL device.

PLL Done: When a one is read, the programmer has successfully completed an input or output request; when a zero is read, this is not the case. This bit is latched and must be cleared by writing the PLL done bit back to this register.

PLL Error: When a one is read, an error occurred while processing a read or write request; when a zero is read, no error occurred.

HLNK_BASE_PLL_FIFO

[0x00C] PLL Output FIFO Write/ PLL Input FIFO Read

PLL Output/Input FIFO Ports

Data Bit	Description
31-0	FIFO data word

FIGURE 7 PMC-HOTLINK BASE PLL FIFO PORT

Writes to this port load PLL programming data into the PLL TX FIFO. This data is used to configure the PLL device. Reads from this port return data from the PLL RX FIFO. This data is the PLL device's internal register data that was read by the PLL programmer. Both FIFOs are 32 words deep and 32 bits wide.

HLNK_CHAN_CNTRL_0

[0x020] Channel Control (read/write)

Channel Control Register

Data Bit	Description
31	Spare
30	Received Frame Read Done Interrupt Enable
29	Read Count Interrupt Enable
28	Read Count Clear Enable
27	RX FIFO Not Almost Full Interrupt Enable
26	TX FIFO Not Almost Empty Interrupt Enable
25	Receiver Start Mode
24	Transmitter Send Frame
23	Send Frame Auto-Clear Enable
22-21	Receiver Storage Mode
20	Receiver Reframe Enable
19	Receiver BIT Enable
18	Receiver A Input Select
17	Transmitter Load Enable
16	Transmitter Output Enable
15	Transmitter BIT Enable
14	Receiver Enable
13	Transmitter Enable
12	Transmit Mode Select
11-10	Spare
9	Read DMA Interrupt Enable
8	Write DMA Interrupt Enable
7	RX FIFO Overflow Interrupt Enable
6	RX FIFO Almost Full Interrupt Enable
5	TX FIFO Almost Empty Interrupt Enable
4	Force Interrupt
3	Master Interrupt Enable
2	FIFO Data Loop-Back Test Enable
1	Receive FIFO Reset
0	Transmit FIFO Reset

FIGURE 8 PMC-HOTLINK CHANNEL CONTROL REGISTER

All bits are active high and are reset on system power-up or reset. If an external control or status bit is active low, it is inverted from the value in this register.

Transmit / Receive FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO and control and status circuitry will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are synchronous, referenced to the PCI clock.

FIFO Data Loop-Back Test Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without sending data through the HOTLink interface. When this bit is zero, normal FIFO operation is enabled.

Master Interrupt Enable: When this bit is set to a one all enabled interrupts for the channel (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one a system interrupt will occur provided the channel master interrupt enable is set. This is useful to test interrupt service routines.

TX FIFO Almost Empty Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level becomes less than the value specified in the HLNK_CHAN_TX_AMT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register and the interrupt will be routed to the base level where it can be configured to cause an interrupt on INTB-D.

RX FIFO Almost Full Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level becomes greater than the value specified in the HLNK_CHAN_RX_AFL register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register and the interrupt will be routed to the base level where it can be configured to cause an interrupt on INTB-D.

RX FIFO Overflow Interrupt Enable: When this bit is set to a one, an interrupt will be generated when an attempt is made to write to a full receive FIFO, provided the channel master interrupt enable is asserted. When a zero is written to this bit, an interrupt will not be generated when an overflow condition occurs, but the latched status can still be read from the channel status register and the interrupt will be routed to the base level where it can be configured to cause an interrupt on INTB-D.

Write / Read DMA Interrupt Enable: These two bits, when set to one, enable the DMA arbiter to use the TX almost empty and/or RX almost full status to give priority to a channel that is approaching the limits of its FIFOs. The levels written to the TX almost empty and RX almost full registers are used to determine these status values. When these bits are zero normal round-robin arbitration is used to determine access to the PCI bus for DMA transfers.

Transmit Mode Select: This bit, when set to one, enables transmitter data-only operation. In this mode the transmit state-machine, if enabled, will read the transmit FIFO and send only data bytes until the transmit data is exhausted. When this bit is zero, the transmit state-machine, when enabled, simulates the target system operation by sending 128 lines of 128 16-bit pixels followed by 96 NULL bytes each as described in the Theory or Operation section above.

Transmitter Enable: This bit, when set to one, enables the HOTLink transmitter state-machine. The behavior of the transmitter depends on the state of the Test Mode bit described above, whether there is data in the FIFO and whether the Send Frame control bit is set. When this bit is zero, the transmitter state-machine is disabled.

Receiver Enable: This bit, when set to one, enables the HOTLink receiver state-machine. The behavior of the HOTLink receiver depends on the Receive Storage Mode 2-bit control field. In the data-only mode the receiver ignores control characters and stores only data bytes. Four bytes are loaded into a 32-bit long-word starting with the least significant byte and written to the receive FIFO. If a 32-bit word is not completed when the receiver is disabled, the remaining unfilled byte positions will be set to zero and the word will be written to the FIFO. In store-all or compact mode, control characters are stored as well as data. Three characters are stored in a 32-bit word with the first character stored in bits 0-9, the second character in bits 10-19 and the third character stored in bits 20-29. The compact mode doesn't store repeated control characters. When this bit is zero, the receiver state-machine is disabled.

Transmitter BIT Enable: This bit, when set to one, enables the HOTLink transmitter Built-In-Test mode. When this bit is zero, Built-In-Test mode is disabled.

Transmitter Output Enable: This bit, when set to one, enables the external output of the HOTLink transmitter. When this bit is zero, only the internal output, which is always on, is enabled.

Transmitter Load Enable: When the Built-In-Test mode is enabled, setting this bit to a one starts the test sequence. This bit is zero in normal operation.

Receiver A Input Select: This bit, when set to one, selects input A of the HOTLink receiver. This input is driven by the transformer-coupled external input. When this bit is zero, input B is selected. This input is driven by the internal signal coming from the channel's HOTLink transmitter output C.

Receiver BIT Enable: This bit, when set to one, enables the HOTLink receiver Built-In-Test mode. When this bit is zero, Built-In-Test mode is disabled.

Receiver Reframe Enable: This bit, when set to one, asserts the HOTLink RF (reframe) control line. This causes the HOTLink receiver chip to search for a comma character to align the serial bit-stream on a byte boundary. When this bit is zero, the RF control signal to the HOTLink receiver chip will not be asserted.

Receiver Storage Mode: This two-bit field controls which received characters are stored in the receive FIFO and how the FIFO word is formatted. When this field is set to "01", only data characters will be stored using eight bits per character and each FIFO word will contain four data-bytes; when this field is set to "00", ten bits will be used to represent a character, all control and data characters will be stored and each FIFO word will contain three characters in bits 0-9, 10-19 and 20-29. Bits 30 and 31 are unused and set to zeros. When this field is set to "10", all data characters will be stored, but a control character will only be stored if it differs from the previous character received. Again, ten bits are used to represent a character and each FIFO word will contain three characters.

Send Frame Auto-Clear Enable: When this bit is set to a one, the Transmitter send frame control bit will be automatically cleared when the frame completes. When this bit is zero, the send frame bit must be explicitly cleared.

Transmitter Send Frame: When this bit is set to a one, the transmitter will start sending a data-frame if the FIFO contains data. When this bit is zero, the frame will not be sent.

Receiver Start Mode: When this bit is set to a one, the receiver state-machine will start storing received data without waiting for a start sequence. When this bit is zero, the state-machine waits for the start sequence (K28.5, K28.4) before storing received data.

TX FIFO Not Almost Empty Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level becomes greater than the value specified in the HLNK_CHAN_TX_AMT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register and the interrupt will be routed to the base level where it can be configured to cause an interrupt on INTB-D.

RX FIFO Not Almost Full Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level becomes less than the value specified in the HLNK_CHAN_TX_AMT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register and the interrupt will be routed to the base level where it can be configured to cause an interrupt on INTB-D.

Read Count Clear Enable: When this bit is set to a one, the read DMA word-counter will be cleared when a read DMA is initiated. When this bit is zero, the word-counter will not be cleared.

Read Count Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the read DMA word-counter matches the count stored in the HLNK_CHAN_READ_COUNT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register and the interrupt will be routed to the base level where it can be configured to cause an interrupt on INTB-D.

Received Frame Read Done Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the last word of a video frame is read from the RX FIFO, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register and the interrupt will be routed to the base level where it can be configured to cause an interrupt on INTB-D.

HLNK_CHAN_STATUS_0

[0x024] Channel Status Read/Latch Clear Write

Channel Status Register

Data Bit	Description
31	Channel Interrupt Active
30	User Interrupt Active
29	Received Frame Read Done Interrupt Active
28	Received Frame Done
27	Read-Count Match Interrupt Active
26	RX FIFO Not Almost Full Interrupt Active
25	TX FIFO Not Almost Empty Interrupt Active
24	Transmit Frame Done
23	RS-485B Framing Error
22	RS-485B Interrupt Active
21	RS-485A Framing Error
20	RS-485A Interrupt Active
19	Transmit Data Read
18	Receive Data Ready
17	Read DMA Ready (Idle)
16	Write DMA Ready (Idle)
15	Read DMA Error
14	Write DMA Error
13	Read DMA Complete
12	Write DMA Complete
11	Receive Symbol Error
10	Receive FIFO Overflow
9	RX FIFO Almost Full Interrupt Active
8	TX FIFO Almost Empty Interrupt Active
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Transmit Data Valid
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 9 PMC-HOTLINK CHANNEL STATUS REGISTER

Transmit FIFO Empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data-words in the transmit data FIFO is less than the value written to the HLNK_CHAN_TX_AMT register; when a zero is read, the level is equal to or more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Transmit Data Valid: When a one is read, there is at least one valid transmit data word left. This bit can be set even if the transmit FIFO is empty, because there is a one-word pipeline after the FIFO output to feed the transmit I/O or FIFO bypass path. When this bit is a zero, it indicates that there is no more valid transmit data.

Receive FIFO Empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data-words in the receive data FIFO is greater than the value written to the HLNK_CHAN_RX_AFL register; when a zero is read, the level is less than or equal to that value.

Receive FIFO Full: When a one is read, the receive data FIFO for the channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Receive Data Valid: When a one is read, there is at least one valid received data word left. This bit can be set even if the receive FIFO status reports empty, because there is a four-word pipeline after the FIFO output to facilitate a PCI read DMA. When this bit is a zero, it indicates that there is no more valid received data.

TX FIFO Almost Empty Interrupt Active: When a one is read, it indicates that the transmit FIFO data count has become less than the value in the HLNK_CHAN_TX_AMT register. A zero indicates that the FIFO has not become almost empty. This bit is latched and must be cleared by writing to the Status register with a one in this bit position.

RX FIFO Almost Full Interrupt Active: When a one is read, it indicates that the receive FIFO data count has become greater than the value in the HLNK_CHAN_RX_AFL register. A zero indicates that the FIFO has not become almost full. This bit is latched and must be cleared by writing to the Status register with a one in this bit position.

Receive FIFO Overflow: When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. If the interrupt enable for this condition has been asserted, this condition will cause an interrupt. A zero indicates that no overflow condition has occurred. This bit is latched and must be cleared by writing to the Status register with a one in this bit position.

Receive Symbol Error: This is a latched version of the RVS (Received Violation Symbol) signal from the channel's HOTLink receiver. This bit is intended to be used for Built-In-Test operation as it indicates an error during the test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Write/Read DMA Complete: When a one is read, it indicates that a corresponding DMA descriptor list has completed. These bits are latched and must be cleared by writing the same bit back to this channel status port. A zero indicates that a corresponding DMA descriptor list has not completed since the bit was last cleared.

Write/Read DMA Error: When a one is read, it indicates that an error has occurred while the corresponding DMA was in progress. This could be a target or master abort or an incorrect direction bit in one of the DMA descriptors. These bits are latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no DMA error has occurred.

Write/Read DMA ready (Idle): These two bits report the DMA state-machine status. If a one is read, the corresponding DMA state-machine is idle and available to start a transfer. If a zero is read, the corresponding DMA state-machine is currently processing a data transfer.

Receive Data Ready: This is a latched version of the /RDY (ready) signal from the channel's HOTLink receiver, which indicates that a character (other than a NULL) is available to be read from that device. This bit can be used for Built-In-Test operation as the ready signal will pulse once per test loop, so polling this bit will indicate the completion of the receive test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Transmit Data Read: This is a latched version of the /RP (read pulse) signal from the channel's HOTLink transmitter. Similarly to the ready bit above, this bit can be used for Built-In-Test operation as the data read signal will pulse once per test loop, so polling this bit will indicate the completion of the transmit test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

RS-485A/B Interrupt Active: When a one is read, it indicates that the corresponding RS-485 state-machine has completed its operation since the bit was last cleared. A zero indicates that this has not occurred. This bit is latched and must be cleared by writing the same bit back to the channel status port.

RS-485A/B Framing Error: When a one is read, it indicates that the RS-485 receiver state-machine has detected a framing error since the bit was last cleared. A framing error occurs if the 33rd bit (stop-bit) of a transmitted word is high. A zero indicates that this has not occurred. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Transmit Frame Done: When a one is read, it indicates that the transmitter has completed a requested transfer. A zero indicates that the transmitter has either not completed a requested transfer or no transfer was initiated.

TX FIFO Not Almost Empty Interrupt Active: When a one is read, it indicates that the transmit FIFO data count has become greater than the value in the HLNK_CHAN_TX_AMT register. A zero indicates that the FIFO has not become not almost empty. This bit is latched and must be cleared by writing to the Status register with a one in this bit position.

RX FIFO Not Almost Full Interrupt Active: When a one is read, it indicates that the receive FIFO data count has become less than the value in the HLNK_CHAN_RX_AFL register. A zero indicates that the FIFO has not become not almost full. This bit is latched and must be cleared by writing to the Status register with a one in this bit position.

Read-Count Match Interrupt Active: When a one is read, it indicates that the read DMA word-counter has matched the count stored in the HLNK_CHAN_READ_COUNT register. A zero indicates that the read DMA word-counter has not matched this count. This bit is latched and must be cleared by writing to the Status register with a one in this bit position.

Received Frame Done: When a one is read, it indicates that a received video-frame has completed since this status bit was last cleared. A zero indicates that a received video-frame has not completed.

Received Frame Read Done Interrupt Active: When a one is read, it indicates that the last video-frame has been completely read from the receiver data FIFO. A zero indicates that the frame has not been completely read.

User Interrupt Active: When a one is read, it indicates that an enabled user interrupt condition (other than the DMA interrupts) is active for the channel. A zero indicates that no enabled interrupt condition is active.

Channel Interrupt Active: When a one is read, it indicates that the interrupt is active for the channel. A zero indicates that the channel interrupt is not active.

HLNK_CHAN_FIFO_0

[0x028] TX FIFO Write/RX FIFO Read

RX and TX FIFO Ports	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 10 PMC-HOTLINK CHANNEL RX/TX FIFO PORT

These ports are used to make single-word accesses into the channel transmit FIFO and out of the channel receive FIFO.

HLNK_CHAN_WR_DMA_PNTR_0

[0x02C] Input DMA Control (write only)

Input DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 11 PMC-HOTLINK CHANNEL WRITE DMA POINTER PORT

This write-only port is used to initiate a scatter-gather input DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values.

HLNK_CHAN_TX_FIFO_COUNT_0

[0x02C] TX FIFO Word Count (read only)

TX FIFO Data Count	
Data Bit	**Description**
31-12	Spare
11-0	TX data words stored

FIGURE 12 PMC-HOTLINK CHANNEL TX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding transmit FIFO. There is an additional latch that may contain data if enabled, which allows this value to be a maximum of 0x10001.

HLNK_CHAN_RD_DMA_PNTR_0

[0x030] Output DMA Control (write only)

Output DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 13 PMC-HOTLINK CHANNEL READ DMA POINTER PORT

This write-only port is used to initiate a scatter-gather output DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values.

HLNK_CHAN_RX_FIFO_COUNT_0

[0x030] RX FIFO Word Count (read only)

RX FIFO Data Count	
Data Bit	**Description**
31-12	Spare
11-0	RX data words stored

FIGURE 14 PMC-HOTLINK CHANNEL RX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding receive FIFO. There are four additional latches in the read DMA pipeline that may contain data, which allows this value to be a maximum of 0x10004.

HLNK_CHAN_TX_AMT_0

[0x034] TX FIFO Almost Empty Level (read/write)

TX FIFO Almost Empty Level Register	
Data Bit	**Description**
31-16	Spare
15-0	TX FIFO almost empty level

FIGURE 15 PMC-HOTLINK CHANNEL TX FIFO AMT LEVEL REGISTER

These read/write ports access the transmitter almost-empty level registers for the channel. When the number of data words in the transmit data FIFO is equal or less than this value, the almost empty status bit is set and an interrupt may be generated if it is enabled.

HLNK_CHAN_RX_AFL_0

[0x038] RX FIFO Almost Full Level (read/write)

RX FIFO Almost Full Level Register

Data Bit	Description
31-16	Spare
15-0	RX FIFO almost full level

FIGURE 16 PMC-HOTLINK CHANNEL RX AFL LEVEL REGISTER

These read/write ports access the receiver almost-full level registers for the channel. When the number of data words in the receive data FIFO is equal or greater than this value, the almost full status bit is set and an interrupt may be generated if it is enabled.

HLNK_CHAN_485_CNTRL_0

[0x03C] Channel RS-485 Control (read/write)

Channel RS-485 Control Register

Data Bit	Description
31-26	Spare
25	RS-485B TX Load Enable
24	RS-485B I/O Enable
23-21	Spare
20	RS-485B Interrupt Enable
19	RS-485B Start/Load Clear Enable
18	RS-485B Direction (1=Transmit, 0=Receive)
17	RS-485B Termination Enable
16	RS-485B FIFO Reset
15-10	Spare
9	RS-485A TX Load Enable
8	RS-485A I/O Enable
7-5	Spare
4	RS-485A Interrupt Enable
3	RS-485A Start/Load Clear Enable
2	RS-485A Direction (1=Transmit, 0=Receive)
1	RS-485A Termination Enable
0	RS-485A FIFO Reset

FIGURE 17 PMC-HOTLINK CHANNEL RS-485 CONTROL REGISTER

All bits are active high and are reset on system power-up or reset.

RS-485A/B FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are referenced to the PCI clock; two periods are required for proper reset.

RS-485A/B Termination Enable: When this bit is set to a one, the parallel termination for the selected RS-485 I/O line will be switched in. When a zero is written to this bit, the corresponding parallel termination will remain open.

RS-485A/B Direction (1=Transmit, 0=Receive): When this bit is set to a one, the selected RS-485 I/O line will be configured as a transmitter. When a zero is written to this bit, the selected RS-485 I/O line will be configured as a receiver.

RS-485A/B Start/Load Clear Enable: When this bit is set to a one, the I/O enable and TX load enable bits will be cleared when the state-machine completes its current data reception or data transmission operation. When a zero is written to this bit, the enable bits will not be cleared on completion, but the interrupt status bit will still be latched.

RS-485A/B Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the selected state-machine completes its current data reception or data transmission operation, provided the channel master interrupt enabled is asserted. When a zero is written to this bit, an interrupt will not be generated, but the latched status can still be read from the channel status register.

RS-485A/B I/O Enable: When this bit is set to a one, the referenced state-machine is enabled. If the direction bit is set to one, the transmit state-machine is enabled and if the direction bit is zero, the receive state-machine is enabled. When a zero is written to this bit, neither state-machine is enabled.

RS-485A/B TX Load Enable: When this bit is set to a one and the selected RS-485 I/O line is configured as a transmitter, data loading from the corresponding FIFO is enabled. When a zero is written to this bit or the selected RS-485 I/O line is configured as a receiver, data present in the corresponding FIFO will not be read and loaded into the I/O state-machine.

HLNK_CHAN_485_STATUS_0

[0x040] Channel RS-485 Status read/Clear write

Channel RS-485 Status Register

Data Bit	Description
31-20	RS-485B FIFO Word Count
19	Spare
18	RS-485B FIFO Data Valid
17	RS-485B FIFO Full
16	RS-485B FIFO Empty
15-4	RS-485A FIFO Word Count
3	Spare
2	RS-485A FIFO Data Valid
1	RS-485A FIFO Full
0	RS-485A FIFO Empty

FIGURE 18 PMC-HOTLINK CHANNEL RS-485 STATUS REGISTER

RS-485A/B FIFO Empty: When a one is read, the referenced RS-485 data FIFO for the channel contains no data; when a zero is read, there is at least one data-word in the FIFO.

RS-485A/B FIFO Full: When a one is read, the referenced RS-485 data FIFO for the channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

RS-485A/B FIFO Data Valid: When a one is read, there is at least one valid RS-485 data word left. This bit can be set even if the RS-485 FIFO is empty, because there is a one-word pipeline after the FIFO output. When this bit is a zero, it indicates that there is no more valid RS-485 data.

RS-485A/B FIFO Word Count: This 12-bit field reports the referenced RS-485 FIFO word count.

HLNK_CHAN_485A/B_FIFO_0

[0x044] RS-485A FIFO (read/write)

[0x048] RS-485B FIFO (read/write)

RS-485A/B FIFO Port	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 19 PMC-HOTLINK CHANNEL RS-485A FIFO PORT

These ports are used to make single-word accesses in and out of the two channel RS-485 FIFOs.

HLNK_CHAN_READ_COUNT_0

[0x04C] Read Count (read/write)

Read-Count Target Port	
Data Bit	**Description**
31-30	Spare
29-0	Read DMA Word-Count

FIGURE 20 PMC-HOTLINK CHANNEL READ-COUNT PORT

This register is used to store the target read-count. This count is compared to the read DMA word-count to generate an interrupt when the target read-count is reached. The read DMA word counter is cleared when a read DMA is initiated, provided the read-count clear enable is asserted. For each 32-bit word transferred by the read DMA, the count is incremented by one. When the target count is reached, if appropriate enables are asserted, an interrupt will be generated.

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-HOTLink. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 21 PMC-HOTLINK PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-HOTLink. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 22 PMC-HOTLINK PN2 INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC-HOTLink Module Pn4. Also, see the User Manual for your carrier board for information on interfacing with Pn4.

HSSIN_0+		1	2
HSSIN_0-		3	4
		5	6
		7	8
		9	10
		11	12
	IO_0+	13	14
	IO_0-	15	16
		17	18
		19	20
		21	22
		23	24
	IO_6+	25	26
	IO_6-	27	28
		29	30
		31	32
		33	34
		35	36
		37	38
		39	40
		41	42
		43	44
HSSOUT_0+		45	46
HSSOUT_0-		47	48
		49	50
		51	52
		53	54
		55	56
		57	58
		59	60
		61	62
		63	64

FIGURE 23 PMC-HOTLINK PN4 INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-HOTLink. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-HOTLink is constructed out of 0.062-inch thick FR4 material.

Through-hole and surface-mount components are used. IC sockets use screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-HOTLink design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. The board is conduction-cooled, therefore low thermal impedance to the carrier cooling rails and surfaces is imperative. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Host Interface (PMC):	PCI Mezzanine Card
Serial Interfaces:	One HOTLink input and one HOTLink output Two RS-485 bi-directional lines
TX Bit-rates generated:	200 MHz for the HOTLink I/O, 500 kHz for the RS-485 I/O Frequencies can be varied by reprogramming the PLL
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	The channel has an interrupt for TX almost empty, RX almost full, RX FIFO overflow, RS-485A/B I/O complete. Read and write DMA interrupts are also implemented for the channel.
DMA:	Independent input and output Scatter/Gather DMA Support implemented for the channel
Onboard Options:	All Options are Software Programmable
Interface Options:	All HOTLink and RS-485 I/O lines are available on Pn4 only
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC-HOTLink	http://www.dyneng.com/pmc_hotlink.html Standard version with two 64K x 32-bit FIFOs, and two 4K x 32-bit FIFOs per channel. Channel I/O on Pn4.
PMC-HOTLink-Eng-1	Engineering Kit for the PMC-HOTLink board-level schematics (PDF)
PMC-HOTLink-Eng-2	Board-level schematics (PDF), Linux Driver and sample application
PMC-HOTLink-Eng-3	Board-level schematics (PDF), Windows Driver and sample application