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Est. 1988

cPCI4IP-MM

User Manual Mini-Map version

Integrated cPCI ⇔ IP Module Carrier

Key Features

Fast Access with integrated PCI ⇔ IP Bridge
4 IP Positions with IO
8/32 MHz IP operation
8/16/32 bit accesses supported
16/32 bit IP module support
Data Alignment – Byte and Word Swapping
Watch Dog Timer
LEDs - Power, IP Access, User
Multi-board support
64K Memory Space for each slot

Manual Revision A
Corresponding Hardware: Revision A 10-2004-0902
Firmware Revision A

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Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

Manual Revision A3 Revised 10/5/07

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Product Description

If **any** of the following applies to you then the cPCI4IP is the right choice for your design. If you are not sure; the questions are close but not quite right please contact Dynamic Engineering for help with your selection. engineering@dyneng.com or sales@dyneng.com can be used to contact Dynamic Engineering staff for pre and post sales support.

Do you need high density IO in your 6U cPCI system?
Do you need mixed IO in your cPCI chassis?
Do you need Windows or Linux support?
Do you want to use IndustryPack® Modules?
Do you need power protection for your system – fused power to the IO?
Do you need trouble free integration?

The cPCI4IP is designed for analog and digital systems including data acquisition, instrumentation, measurement, command/control, telemetry and other industrial applications.

cPCI4IP is part of the Dynamic Engineering IP Compatible family of modular I/O components. The cPCI4IP provides four IndustryPack® Compatible sites in one 6U 4HP cPCI slot. The slot pairs can be used for double wide IP Modules with either 16 or 32 bit IP Module bus.

The –MM version of the cPCI4IP design has minimized memory spaces for each slot to allow the overall memory map to be reduced to 1/8th of the standard product memory requirement. If you do not use the memory space or do not use all of it, 64K may be enough.

Each IP position has 50 lines of IO for a total of 200 IO on the bezel [std] or the backplane [-RP] or both[-IO]. It is even possible to mix rear and front panel IO [customerized].

Each slot has separated, filtered, fused power to allow analog and digital IO in one slot.

Windows and Linux are supported with a layered driver. A generic driver is part of the base driver to support IP's without a native driver.

IndustryPack® Modules are an industry standard with hundreds of models to choose from. IndustryPack® Modules are an optimal size – small enough to be able to put 4 different ones on a 6U board and large enough to support 50 IO each with signal conditioning and logic. The cPCI4IP is compliant with the PCI, cPCI and IP module standards.

IO is supported with cables[HDRcabl50], breakouts [HDRterm50] and test equipment [IP-Debug-IO, IP-Debug-Bus].

With standard compliance, software support, IO support, documentation and customer support Dynamic Engineering has the solution for you. Dynamic Engineering has alternate solutions based on PMC, PCI, PC/104p and other standards.

cPCI4IP Rear Panel IO version shown

Details

ID, IO, INT, and MEM access types are supported for read and write cycles. The full 8 Mbytes of address space is not allocated, 64K is allocated to each of the MEM spaces.

The PCI bus is 32 bits wide and most industry packs are 16 bit devices. Byte, word, and long word accesses are supported. Bytes can be to any address. Word accesses need to be word aligned. Long word accesses need to be long word aligned. Each of the access types has a one-to-one correspondence to the hardware. There are no "extra" accesses with the cPCI4IP design.

The Data bus is designed as a 32-bit bus with slot B,D on the D15-0 segment. A and C are on the D31-16 half of the bus. The hardware compensates and allows for standard accesses to all slots – software transparent. The AB and CD slots can be accessed as a 32 bit wide data path. The AB and CD slots are mechanically aligned for double wide card installation as well as pairs of single wide cards.

A long word access to a 16 bit port will automatically be converted into two back-to-back IP accesses with the address incrementing between cycles unless the increment disable function is selected (see Slot control register description). In the increment disable case the hi or low address can be specified for the double access.

For a read, one 32 bit data word will be returned. For example a long word read to the ID space would yield $xx50xx49 for many boards as the "0" location has $49 and the next address has $50. The long word mode happens automatically when all 4 of the byte lane enables are detected asserted. The overall throughput is greatly enhanced with this mode of operation. Please note that the non-data bytes should be masked, as many IPs do not drive the “off byte”.

For a long word access to a long word port the 32 bit IP data bus is utilized. Positions AB and CD form a 32 bit slot when 32 bit IPs are installed. The access type is automatic based on the address space used to access the slots. You can use 16 and 32 bit accesses intermixed without changing your control registers if the IP supports both. Slot B/D control register defines the access when in 32 bit mode. It may be necessary to match Slot A/C clock to slot B/D if your IP uses both.

The address is shifted from long [32] to short [16] by hardware and the byte strobes used to access the individual bytes or words. If your card has mixed addressing requirements you may need dual defines to account for the 32 bit and 16 bit addressing.

The PCI bus is defined as little endian and many IPs have their register sets defined to operate efficiently with a little endian interface. The default settings on the cPCI4IP are “straight through” byte for byte and D15-0 written to address 0x00 before D31-D16

written to address 0x02 when long words are written to 16 bit ports. Please note that any long word address can be used. The lower data is written to the lower address first, then the upper data to the upper address. Each slot has a BS and WS control bit to allow Byte and Word Swapping to be performed to accommodate alternate IP and OS requirements.

Byte Swapping
16 bit ports
D15-8 ⇔ D7-0
D31-24 ⇔D23-16
32 bit ports
D31-24 => D7-0
D23-16 => D15-8
D15-8 => D23-16
D7-0 => D31-24

Word Swapping will swap D31-16 with D15-0

If byte swapping is enabled and 0x1234 is written to an IP slot, then the IP will see 0x3412. If 0x12345678 is written to a 32-bit port then the IP will see 0x78563412. The "is written" is defined by the data on the PCI bus. Your software/OS may do its own conversion before the data gets to the PCI bus.

The byte and word swap controls are separated to allow the conversion to be used for big-little endian and for register mapping purposes. Each slot has separate controls for access to that slot.

The cPCI4IP has a watch-dog timer function which completes the IP access if the IP does not respond within 7.6 uS. The watch-dog timer has a master status bit and an optional interrupt output. In addition to the master status each slot control register reports status for the bus error. Multi-threaded programs can tell if their hardware access caused the Bus Error even if other threads have accessed other hardware since the bus error was caused.

Each slot is programmable for 8 or 32 MHz. operation. The control register has separate bits for slots A, B, C, and D. The clocks are locked together and can be switched at any time. Hardware insures that the clocks switch basis on a clock period boundary to provide seamless operation.

The cPCI4IP supports interrupts from each slot with separate mask bits. Two interrupts from each of the slots. An interrupt "force" bit is supplied to aid in software development. The bus error [watch dog timer] can also be an interrupt condition. The masked interrupts are tied together and connected to INTA on the PCI bus.

The cPCI4IP has LED's for power, access, and user functions. The three voltages from slot D are connected to three LED's. An additional 8 LED's are supplied which are controlled via the control register for user defined purposes. Four LEDs are controlled by a timer circuit which is activated by the acknowledge from each of the IP slots.

The power to each of the IP slots is individually filtered and fused for +5 and ±12. The fuses are rated at 2A on the 5V rail and 1.1A on the ±12V rails. The cPCI4IP is designed to route maximum power to each slot in parallel. The power supply capabilities for your chassis may provide additional constraints. Each slot filter has a separate RF filter, bulk capacitor, “self healing” fuse, and bipass capacitors. A bipass capacitor is located at each of the power pins on the CPCI4IP with the bulk capacitor near the filter pin for optimum noise rejection, voltage hold-up and local filtering.

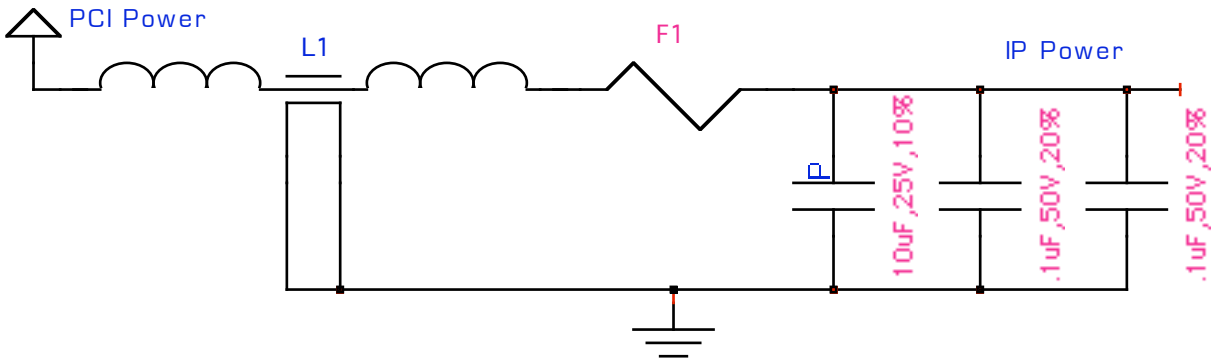


FIGURE 1 CPCI4IP POWER FILTERING

With the filter pin on each slot and bulk capacitor each IP is effectively isolated from the other IPs mounted to the cPCI4IP. Additional work was done in layout to minimize the amount of cross-slot electronic noise. Each of the IP slots is also isolated from the PCI interface by the power conditioning. The FPGA uses 3.3 and 2.5V power. The 2.5V is derived from the 5V supply and bussed on mini-planes to the FPGA. The FPGA is effectively isolated from the IP slots by the regulator and additional filtering.

The cPCI4IP is well behaved with low noise power provided to each of the slots. The cPCI4IP is designed for analog and digital IP Module based systems including data acquisition, instrumentation, measurement, command and control, telemetry and other industrial applications.

The IO is routed with matched length for each slot.
An 8 bit "dip switch" is provided on the cPCI4IP. The switch configuration is readable via a register. The switch is for user defined purposes. We envision the switch being used for software configuration control, PCI board identification or test purposes. The

Dynamic Engineering Driver uses the switch to identify multiple carriers of the same type within a system.

The reset switch provided can be used to reset the IP devices without affecting the PCI bus. Power, PCI reset, and a control register bit also cause the IP Reset to be activated. The reset is controlled to be synchronous to the 8 MHz. clock. Alternatively, the IP-Debug-Bus card can be used for individual slot resets.

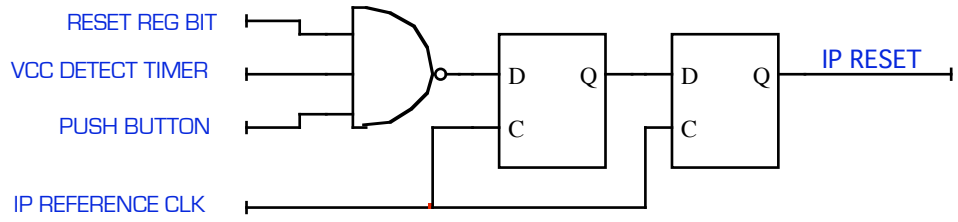


FIGURE 2 CPCI4IP RESET CIRCUIT

The cPCI4IP conforms to the VITA standard for IndustryPack Carriers. This guarantees compatibility with multiple IndustryPack compatible modules.

The cPCI4IP conforms to the PCI 2.3 specification and supports both 3.3V and 5V signaling levels. The cPCI4IP is accessible in the memory space on the PCI bus. This guarantees compatibility with other cPCI compliant hardware.

The cPCI4IP is compatible with PICMG 2.4 R 1.0 for the IO definitions when J4 and J5 are installed.

The PCI interface is integrated with the IP interface providing superior performance over designs relying on a separate PCI interface device. In addition to access speed the higher level of integration results in fewer initialization steps and requirements, more flexibility in operation, a higher MTBF, and less complex software.

If your project can benefit from a "non-standard" implementation, or features that we have not implemented yet please let us know. The Xilinx has room.

Wired but not yet implemented. (1) All of the DMA control signals are available for a future revision to implement.

Wired and User implemented. The IP Strobe signal is connected from each IP slot to a header to allow for inter-slot user defined communications. The IP specification does not define what the strobe can be used for. The header is rarely used. If you need it please add –stb to your order number and we will install the header for you. Standard

.025” sq. posts suitable for wire-wrap inter-connection.

On the IP Slot the Strobe signal is connected to pin 46.

Strobe Pinout on Header

J8	
1	STB A
2	STB B
3	STB C
4	STB D

FIGURE 3 CPCI4IP STROBE CONNECTION TABLE

The IO are brought to 50 pin headers [default]. The headers are installed with ejectors for ease of use and retention. The IO are also optionally available at the rear panel [-RP]. The rear panel IO are isolated with 0Ω resistors located near the IP-IO connectors to minimize the stub length if the rear panel IO is not in use. If using rear panel IO the front bezel has a blank installed for better EMI sealing. The –IO option provides both Bezel and J4/J5 IO.

Theory of Operation

The cPCI4IP is used to bridge from cPCI to IP bus specifications. The cPCI bus will be the master in most cases with the IP's being accessed for read or write cycles. The cPCI accesses are handled at the lowest level by the PCI core.

The cPCI bus provides multiplexed address and data plus control lines. The data is separated from the address, and the control lines are decoded to provide the inputs to the IP Interface state machines. The address is tested to determine which slot the access belongs to and which type of access to implement. The IP control strobes are generated. When acknowledge is received the cycle is terminated back to the host. The PCI bus will see a retry mode while the access is taking place and "disconnect with data" when the cycle is completed.

Feature List

• cPCI Universal Voltage [3.3 or 5V signaling]
• Integrated PCI ⇔ IP conversion for faster access
• 4 IP compatible slots
• Full ID, IO, INT, and 64K of Memory space allocated for each slot
• 8 or 32 MHz operation in each slot independently
• byte, word, long word access. 32 bit access to 16 bit slots with static or incrementing address. 32 bit access to 32 bit slots.
• byte and word swapping for little endian – big endian conversion
• Bus error abort response with slot status
• Bezel IO 1:1 50 pin headers
• J4/J5 IO option with isolation resistors. Matched length routing from each slot.
• IP Reset Switch
• 8 position "DIP Switch" – slot identification for multiple cPCI4IPs
• 8 User LEDs, 3 Power LEDs, 4 Access LEDs
• Fused Filtered Power with re-settable “self healing” fuses in each slot.
• Upgrade Program. Get the newly added features with a new PROM.
• Fully compliant injector/ejector handle on cPCI EMC bezel.
• ESD strip per cPCI specifications.
• Windows®XP and 2000 Drivers available. Generic IP interface included with driver to support your IP. Dynamic Engineering driver development available for customized IP support.
• Linux Driver can be ported from PCI5IP design.
• Plug and Play operation with Addressing, Interrupts, driver loading for Windows® and other O/S. Manuals available on cPCI4IP web page.

The drivers are organized as “Parent” and “Child”. The parent drivers are unique to each of the Dynamic Engineering carriers. The Child drivers are portable between any of the Dynamic Engineering carriers. Develop on the PCI3IP and then reuse on the cPCI4IP for example. The portability applies to the Windows and Linux drivers.

As Dynamic Engineering adds features to the hardware we will update the cPCI4IP page on the Dynamic Engineering website. If you want the new features, and have already purchased hardware, we will support you with a PROM update. We will ship a new PROM with the updated program to you for shipping plus $25 per PROM. If you are interested please send a PO with shipping instructions, the serial numbers of the boards to upgrade and the programming charge.

The basic PCI identifying information will not change with the updates. The revision field will change to allow configuration control. Current revision is 0x01.

Installation

The cPCI4IP and the IPs to be mounted should be treated as static sensitive hardware. The technician should be properly grounded; the mounting and installation process should be performed at a static free workstation.

The cPCI4IP can be installed into any cPCI slot with 6U 4HP capability. The bezel securely retains the cPCI4IP within the chassis. The cPCI4IP with type1 IP Modules installed is cPCI legal for height, length and width. Adjacent slots can be filled with multiple cPCI4IP cards. With Type II modules, [parts on the rear] in most cases, the combination will still be “single slot”.

Each of the IP slots can have an IP installed. IndustryPack®s are installed by pushing the mezzanine card onto the connector pair on the cPCI4IP. Each slot is clearly marked. The IO connector is located near the top of the cPCI4IP and the IP Bus connector near the cPCI backplane connectors. The IP connectors are keyed making orientation error proof. Please refer to Figure 13 for the slot and IO connector placement.

The IP mounting kit can be utilized to secure the IP to the cPCI4IP. Each Dynamic Engineering IP sold comes with a mounting kit. If you need a replacement or your IP comes from another manufacturer please order IP-MTG-HW. 1 kit per IP. The kit includes stainless steel hardware – screws and standoffs.
http://www.dyneng.com/IPHardware.html

If more than one cPCI4IP is to be installed into the same system – visible on the PCI bus then the dipswitch can be set to different positions on each card. The software can use the dipswitch setting to identify which cPCI4IP is allocated which address space and associate specific IP/cables with that cPCI4IP so there is positive automatic control of your system configuration. The Dynamic Engineering Driver makes use of this feature to allow multiple cPCI4IPs to be used in the same system without identification challenges.

Address Map

```
cPCI4IP_intreg_base     0x00000000 // base control register
cPCI4IP_intreg_a        0x00001000 // slot A specific clock and interrupt
cPCI4IP_intreg_b        0x00002000 // slot B
cPCI4IP_intreg_c        0x00003000 // slot C
cPCI4IP_intreg_d        0x00004000 // slot D
cPCI4IP_intreg_dswitch  0x00006000 // User Switch read back port
cPCI4IP_intreg_int      0x00007000 // Interrupt status read-back

cPCI4IP_ida_st          0x00140000  // starting addr of slot A ID space
cPCI4IP_idb_st          0x00120000  // starting addr of slot B ID space
cPCI4IP_idc_st          0x00150000  // starting addr of slot C ID space
cPCI4IP_idd_st          0x00130000  // starting addr of slot D ID space
cPCI4IP_idab_st         0x00160000  // starting addr of slot AB ID space
cPCI4IP_idcd_st         0x00170000  // starting addr of slot CD ID space

cPCI4IP_ioa_st          0x00240000  // starting addr of slot A IO space
cPCI4IP_iob_st          0x00220000  // starting addr of slot B IO space
cPCI4IP_ioc_st          0x00250000  // starting addr of slot C IO space
cPCI4IP_iod_st          0x00230000  // starting addr of slot D IO space
cPCI4IP_ioab_st         0x00260000  // starting addr of slot AB IO space
cPCI4IP_iocd_st         0x00270000  // starting addr of slot CD IO space

cPCI4IP_inta_st         0x00340000  // starting addr of slot A INT space
cPCI4IP_intb_st         0x00320000  // starting addr of slot B INT space
cPCI4IP_intc_st         0x00350000  // starting addr of slot C INT space
cPCI4IP_intd_st         0x00330000  // starting addr of slot D INT space
cPCI4IP_intab_st        0x00360000  // starting addr of slot AB INT space
cPCI4IP_intcd_st        0x00370000  // starting addr of slot CD INT space

cPCI4IP_mema_st         0x00440000  // starting addr of slot A MEM space
cPCI4IP_mema_en         0x0044FFFF  // end address of slot A MEM space
cPCI4IP_memb_st         0x00420000  // starting addr of slot B MEM space
cPCI4IP_memb_en         0x0042FFFF  // end address of slot B MEM space
cPCI4IP_memc_st         0x00450000  // starting addr of slot C MEM space
cPCI4IP_memc_en         0x0045FFFF  // end address of slot C MEM space
cPCI4IP_memd_st         0x00430000  // starting addr of slot D MEM space
cPCI4IP_memd_en         0x0043FFFF  // end address of slot D MEM space
cPCI4IP_memab_st        0x00460000  // starting addr of slot AB MEM space
cPCI4IP_memab_en        0x0046FFFF  // end address of slot AB MEM space
cPCI4IP_memcd_st        0x00470000  // starting addr of slot CD MEM space
cPCI4IP_memcd_en        0x0047FFFF  // end address of slot CD MEM space
```

FIGURE 4 CPCI4IP ADDRESS MAP

The address map is for the local decoding performed within cPCI4IP. The addresses are all offsets from a base address. The host the cPCI4IP is installed into provides the base address and interrupt level. Your software will need to concatenate the base address + cPCI4IP address + IP Local address to create a pointer to each programmable feature on your IP.

Programming

The address map will get you to the IP. The IP board description will provide the local addresses. If you are in a Windows or Linux environment we recommend utilizing the Dynamic Engineering Driver for the carrier and IP. Complete information is provided within this manual to allow customers who use another OS or want to write their own interface to do so.

Dynamic Engineering can write a driver for your IP to interface with our carrier(s) even if it is not “one of ours”. Please contact engineering@dyneng.com with your requirements if you are interested in this service.

The host system will search the cPCI bus to find the assets installed during power-on initialization. The VendorId = 0x10EE and the CardId = 0x0030 for the cPCI4IP-MM (please note that this is a different CardID than the standard cPCI4IP). Interrupts are requested by the configuration space. PCIView and other third party utilities can be useful to see how your system is configured. The VendorId and CardId parameters are used by the OS to identify the card, and in some cases launch the plug and play installation process. The interrupt level expected and style is also set in the registry.

Once the initialization process has occurred and the system has assigned an address range to the cPCI4IP card, the software will need to determine what the address space is. We refer to this address as base0 in our software.

The next step is to initialize the cPCI4IP. The default of no interrupts enabled and 8 MHz. operation will be valid in many cases. The base register for the cPCI4IP and specific slot registers A,B, C, D can be initialized to change the default parameters to suit your requirements. Please refer to the register map definitions for more information.

Access to your installed IP is done by accessing base0 + slot address + IP offset. The slot address is defined in the memory map. For example to read your IP in slot B IO space: *(base0 + cPCI4IP_iob_st + ip offset) = data. Each slot and memory type [IO, ID, INT, Mem] has a unique address space for multiple defined address spaces plus the cPCI4IP internal address space. The internal registers are defined in the following pages.

The cPCI4IP has an integrated PCI interface with IP bridge. The integrated approach simplifies programming with only one base address and fewer parameters to have to initialize. The integrated approach is also faster access creating higher performance in your system.

Higher performance for your system can be achieved by matching the IP register model

to the OS and user software model that you are using, selecting the optimal IP reference clock rate and access types.

The cPCI4IP has individual clock selection for each of the IP Slots. The access time is reduced when the IP clock rate is set to 32 MHz. The cPCI4IP can handle any mixture of clock requirements. Make sure that the IP in the slot can handle the higher rate.

The cPCI4IP can handle byte, word and long word accesses from the PCI bus. The state machine within the bridge will automatically select16 or 32 bit IP width based on the address space utilized. 32 bit accesses to 16 bit ports will be converted to double accesses. 32 bit accesses to 32 bit ports will be handled in a single access. The Byte Swap [BS], Word Swap [WS], Address Increment, and Word High allow the accesses to be customized for the IP installed for optimum performance. 32 bit accesses to 16 bit ports are faster than individual 16 bit accesses and frequently easier to write software for. For example if your IP has a 24 bit port with 16 bits in one register and 8 in the next you can write all 24 with one 32 bit access. With word and byte swapping you can account for the organization of the registers on the IP. Some IPs convert 16 bit accesses to double 8 bit accesses – IP-QuadUART for example. If your IP has 16:8 conversion then you can write 32 bits and get 4 – 8 bit writes to your IP in one access.

Read the IP manual and see what strategy is best to communicate with that card then adapt the settings on the cPCI4IP to optimize your accesses for that IP.

For higher performance and ease of use Dynamic Engineering recommends using our Window® or Linux drivers. The drivers for the Dynamic Engineering IP carriers take care of the local configuration and provide resources to the overlaying IP drivers. When combined high speed “plug and play” operation results. The carrier level driver comes with a “generic” driver which can be used with any IP and is provided to cover IPs from third parties without a board specific driver. Please contact Dynamic Engineering to write a driver for your IP.

Register Definitions

cPCI4IP_intreg_base

[$00 Main Control Register Port read/write]

CONTROL REGISTER 0

DATA BIT	DESCRIPTION
31	Reset 1 = reset IPs 0 = normal
30-14	spare
13	INT FORCE 1 = FORCE 0 = NORMAL
12	Master INT EN 1 = ENABLED 0 = DISABLED
11	spare
10	spare
9	Bus Error Int/Status Clear
8	Bus Error Int En
7	LED7 1 = ON 0 = OFF
6	LED6
5	LED5
4	LED4
3	LED3
2	LED2
1	LED1
0	LED0

FIGURE 5 CPCI4IP CONTROL PORT

Reset when set causes a reset to the IP slots. Reset is active as long as the Reset signal is asserted.

LED7-0 are the user LED's situated at the center top side of the card near Slot B. Each LED can be activated by setting the corresponding data bit and deactivated by clearing the same bit. The LEDs are aligned 7-0
0x12 would be off off off on off off on off

Spare means undefined.

INT FORCE will, when set, cause INTA on the PCI bus to be asserted. This bit can be useful for software debugging. Set this to simulate an IP interrupt when the hardware is not available. The master interrupt must be enabled to have an effect.

Master Interrupt Enable must be set to allow the IP or other interrupt conditions to become an interrupt on the PCI bus. 1 = enabled. 0 = disabled or masked.

Bus Error Int En when ‘1’ allows the bus error detection circuit to cause an interrupt to the host when a Bus Error is detected. The status is available on the Interrupt status register. When ‘0’ the status is still valid but no interrupt is generated when a bus error is detected. The bus error is detected when an access to one of the IP slots is not responded to by IP hardware within the time-out period of approximately 7.3 uS. The bus error circuit is always enabled and automatically responds as if the IP had responded. The data read will typically be $FF if the IP is not driving the bus for a bus error read. For a bus error write the write should be assumed to not have taken place. The host will not know that the bus error has taken place unless the host checks the status. The interrupt can provide a prompt to check the status during operation. During initialization if the software is checking to “see” what is installed or what address range is valid on an IP then the status can be polled to see if the IP responded.

Bus Error Status / INT Clear when ‘1’ will clear the status bit and interrupt request [if enabled]. The Clear bit needs to be reset to ‘0’ to be able to capture the next Bus Error. The bus error timer hardware operates independent of clearing the status and will continue to monitor and intercede whether the status is read or cleared.

cPCI4IP_intreg_(a-d)

[$1000,2000,3000,4000 Slot Control Register Port read/write]

Slot CONTROL REGISTER (A-D)

DATA BIT	DESCRIPTION
31-18	unused
17	Interrupt Status 1
16	Interrupt Status 0 1= interrupt active
15-10	unused
9	bus error status/clear 32 bit access
8	bus error status/clear 16 bit access
7	word swap control
6	byte swap control
5	Interrupt Enable 1
4	Interrupt Enable 0
3	High Word Access
2	Increment Disable
1	spare
0	Speed Control 1 = 32 MHz, 0 = 8 Mhz

FIGURE 6 CPCI4IP SLOT CONTROL PORT

Speed Control selects the slot clock speed. 1 = 32 MHz. 0 = 8 MHz. Clock selection change can be made at any time. Each slot has a separate speed control bit. Default is 8 MHz.

Increment Disable, when '1', turns off the address increment that normally occurs between 16-bit IP cycles when a 32-bit PCI access is performed. This is useful if, for instance, a FIFO is mapped to a single IP address since it allows double IP accesses to the same address with a single PCI transfer. All types of access are affected (i.e. MEM, IO, INT, and ID). Each slot has independent controls and operation. Only 32 bit accesses are affected.

High Word Access controls which 16-bit word is accessed when the Increment Disable is asserted. When '0' the lower word is accessed twice, when '1' the upper word is accessed twice. This bit only has an effect when the Increment Disable bit is '1'. For correct functioning, please make sure the PCI access is on a long-word boundary.

Interrupt Enable 0,1 individual masks for the 2 interrupts from each of the IP Module slots. 0 corresponds to INT0 and 1 corresponds to INT1.

Byte Swap when '1' causes the byte lanes to be swapped. For a 16-bit access the upper byte is swapped with the lower byte. For a 32-bit access to a 16-bit port the upper and lower of each word are swapped. For a 32-bit access to a 32-bit port the

bytes and words are swapped so D31-24 becomes D7-0 etc. Byte Swap when '0' provides the data on the same byte lanes that the PCI bus provides them on. Byte Swapping can be used with the Word Swap feature for big endian ⇔ little endian conversion.

16 bit ports
D15-8 ⇔ D7-0
D31-24 ⇔D23-16

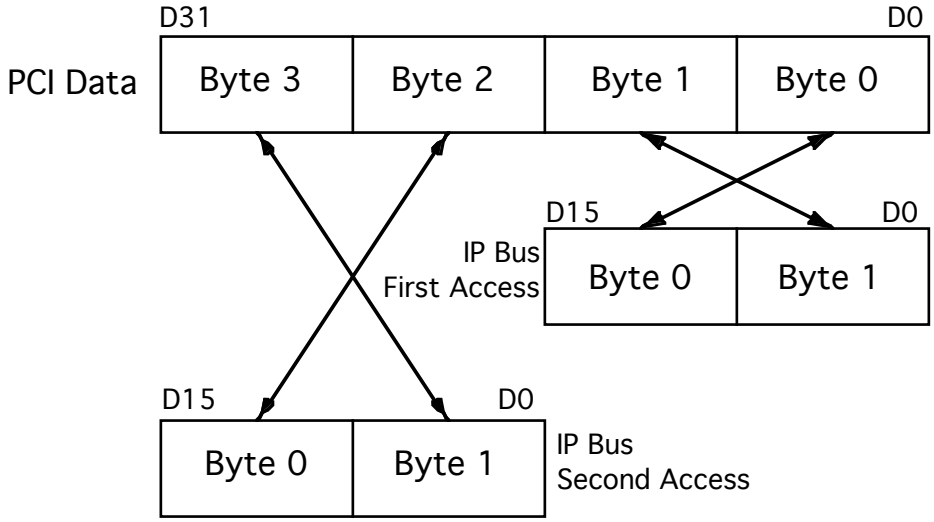


FIGURE 7 CPCI4IP 16 BIT BYTE SWAPPING

32 bit ports
D31-24 ⇔ D7-0
D23-16 ⇔ D15-8
D15-8 ⇔ D23-16
D7-0 ⇔ D31-24

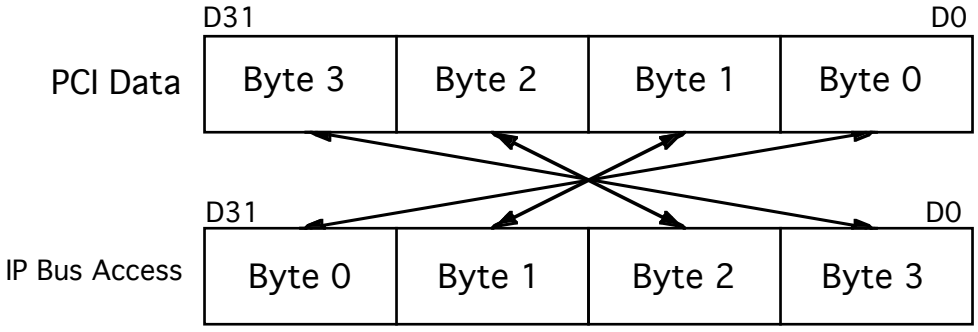


FIGURE 8 CPCI4IP 32 BIT BYTE SWAPPING

Word Swap when ‘1’ will cause the upper and lower words to be swapped. Data written to PCI D15-0 will be driven onto the IP bus as if it originated on D31-16. Word Swap when ‘0’ leaves the data on the PCI word definitions. Please note that Word Swap has no effect on 32 bit accesses to 32 bit IP Module ports.

The IP bus interface state-machine will move data from D15-0 to the “0” address and from PCI D31-16 to the IP “2” address. IP addresses are word based for non-32 bit capable accesses [even with 32 bit transfers]. The PCI bus will write data to either the upper or lower words and apply the corresponding CBE byte lane strobes. The cPCI4IP hardware will translate the data to D15-0 on the IP.

Word swapping can be used effectively for big endian ⇔ little endian translation and to accommodate IPs with registers that can be more effectively accessed in reverse order. For example: if the IP registers are organized with the MS data at address 0x00 and the LS data at 0x02 then a single 32 bit write can be made to 0x00 with address incrementing enabled and word swapping enabled so that the PCI D31-16 data is written to IP 0x00 and the PCI D15-0 data is written to IP 0x02. If the IP registers have data 16 bits or less then word swapping will not be needed.

With the combination of Byte and Word Swapping plus address definition any byte/word can be direct to/from any destination. Big ⇔ little endian issues can be resolved and IP architecture optimized for software access.

The **bus error** bits are status bits with associated write clear. The clear is active at the time of the write only and does not need to be reset. If the bus error bit is set when the register is read, then a bus error has occurred on this slot. Once set, the bit will remain set until explicitly cleared by writing a ‘1’ to this bit position. The 16 bit status should be monitored for “standard” 16 bit IP Modules. The 32 bit status is only active in registers B,D and only has meaning for 32 bit accesses.

Interrupt Status 0, 1: These are read-only status bits indicating, when the bit is a ‘1’, that the corresponding IP interrupt is active. However, the interrupt will not be passed on to the PCI bus unless the respective interrupt enable is also set.

cPCI4IP_intreg_int

[$7000 CPCI4IP interrupt register read only]

CONTROL REGISTER 0

DATA BIT	DESCRIPTION
31-23	undefined
22	Bus Error 1= occurred 0 = none
21	
20	
19	UNMASKED D1
18	UNMASKED D0
17	UNMASKED C1
16	UNMASKED C0
15	UNMASKED B1
14	UNMASKED B0
13	UNMASKED A1
12	UNMASKED A0 1 = SET 0 = NOT SET
11	'0'
10	INTRN 1 = SET, 0 = NOT SET
9	
8	
7	MASKED D1
6	MASKED D0
5	MASKED C1
4	MASKED C0
3	MASKED B1
2	MASKED B0
1	MASKED A1
0	MASKED A0 1 = SET 0 = NOT SET

FIGURE 9 CPCI4IP INTERRUPT STATUS PORT

The interrupt requests from each of the IP slots are available as status from this port. The interrupt requests are inverted to make them active high for software usability. The requests are available in a masked and unmasked form to allow polling with the PCI interrupt masked off. When an interrupt is detected this register should be accessed to determine the source or sources and then appropriate action taken to clear the interrupt at the IP or clear the mask on cPCI4IP.

The cPCI4IP provides direct access to the interrupt space. If the IP causing the interrupt requires an interrupt vector fetch to clear the interrupt then the appropriate INT space should be accessed. Address bit A1 selects between Int0 and Int1. A1 follows the word address to allow access to both INT0 and INT1 clearing addresses within the INT space.

If the IP does not require a Vector fetch then proceed with IO or other accesses as necessary.

The Bus Error status bit is set high when a Bus Error is handled by the internal watch dog timer circuit. The status will stay high until cleared with the Bus Error Int / Status Clear bit in the base control register. The Bus Error status bit is or'd into the interrupt request logic and if enabled will cause a level sensitive interrupt to the host. The interrupt will remain asserted until the status is cleared. The cPCI4IP Base register contains the enable and clear for the bus error logic.

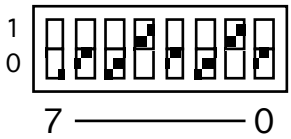
cPCI4IP_intreg_dswitch

[$6000 User Switch Port read only]

DipSwitch Port	
DATA BIT	**DESCRIPTION**
7..0	Sw7..0

FIGURE 10 CPCI4IP USER SWITCH PORT

The user switch is read through this port. The bits are read as the lowest byte. Access the port as a long word and mask off the undefined bits. Read only. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Start-up Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID 0x10EE and CardId 0x0030 and an interrupt level. Look quickly! If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all be connected to a common point.

Power control and static electricity. As the internal dimensions of integrated circuits continues to shrink the susceptibility to static damage increases. Treat the cPCI4IP and IP Modules as static sensitive to insure long life within your system.

Consider the power flow within your system and make sure that un-powered equipment will not be subjected “reverse energising” from active signals when the power is off. The easiest way to deal with this is to turn all of the equipment on and off together. When your equipment is part of a larger system that can’t be powered down then isolation or IO types that allow for hot connection should be employed on the IPs installed onto the cPCI4IP.

Connector definition. The cPCI4IP has two IO options. The front panel IO is provided with a “condo” header; two 50 pin ribbon cable connectors stacked. The ribbon cable connectors have ejectors which are handy for retention and cable removal.

The IO can also be accessed via the J4/J5 connector on the cPCI bus. When the rear IO is not installed the IO is isolated by removing the J4/J5 connectors and not installing the isolation resistors. The isolation resistors are located near the front panel IO to minimize the unused trace length when using the front panel IO. The standard version has the front panel IO installed [only]. The –RP option adds in the J4 and J5 connectors and isolation resistors.

Please refer to the connector definition tables for pin-outs. The front panel IO is 1:1 with

standard ribbon cable definitions. The rear panel IO [J4/J5] follows the cPCI specification [PICMG® 2.4 R1.0.]

Engineering Kit

Dynamic Engineering provides Engineering Kits to help our customers have a successful and quick integration. Engineering Kits will save time and money with decreased T&I. We recognize that different customers have different needs. The Engineering Kits are standardized in description to help with selection. The kits are segmented to allow for customers who only need hardware support, software support or a mixture. The Engineering Kit is highly recommended for first time buyers. The kit pricing is discounted to encourage their use.

cPCI4IP-Eng-1 ..... Hardware Support Engineering Kit includes:
Board level Schematics [PDF], IP-Debug-Bus, IP-Debug-IO.

cPCI4IP-Eng-2 ..... Hardware Support plus Driver Engineering Kit includes: Board level Schematics [PDF], Software[cPCI4IP Driver and sample application zip file], IP-Debug-Bus, IP-Debug-IO.

cPCI4IP Drivers..... Software Support Only Windows®XP and 2000 compliant drivers for the cPCI4IP. The driver is designed to be overlayed with individual IP Module(s) driver(s). Please see the Driver manual for the specifics of writing your board interface. Please contact Dynamic Engineering if you would like us to produce one for your IP or a third party design.

J4 IP Module IO Pin Assignment

AIO	J4	BIO	J4
1	A11	1	A25
2	B11	2	B25
3	C11	3	C25
4	D11	4	D25
5	E11	5	E25
6	A10	6	A24
7	B10	7	B24
8	C10	8	C24
9	D10	9	D24
10	E10	10	E24
11	A9	11	A23
12	B9	12	B23
13	C9	13	C23
14	D9	14	D23
15	E9	14	E23
16	A8	16	A22
17	B8	17	B22
18	C8	18	C22
19	D8	19	D22
20	E8	20	E22
21	A7	21	A21
22	B7	22	B21
23	C7	23	C21
24	D7	24	D21
25	E7	25	E21
26	A6	26	A20
27	B6	27	B20
28	C6	28	C20
29	D6	29	D20
30	E6	30	E20
31	A5	31	A19
32	B5	32	B19
33	C5	33	C19
34	D5	34	D19
35	E5	35	E19
36	A4	36	A18
37	B4	37	B18
38	C4	38	C18
39	D4	39	D18
40	E4	40	E18
41	A3	41	A17
42	B3	42	B17
43	C3	43	C17
44	D3	44	D17
45	E3	45	E17
46	A2	46	A16
47	B2	47	B16
48	C2	48	C16
49	D2	49	D16
50	E2	50	E16

FIGURE 11 CPCI J4 PIN ASSIGNMENT

J5 IP Module IO Pin Assignment

CIO	J5	DIO	J5
1	A11	1	A22
2	B11	2	B22
3	C11	3	C22
4	D11	4	D22
5	E11	5	E22
6	A10	6	A21
7	B10	7	B21
8	C10	8	C21
9	D10	9	D21
10	E10	10	E21
11	A9	11	A20
12	B9	12	B20
13	C9	13	C20
14	D9	14	D20
15	E9	14	E20
16	A8	16	A19
17	B8	17	B19
18	C8	18	C19
19	D8	19	D19
20	E8	20	E19
21	A7	21	A18
22	B7	22	B18
23	C7	23	C18
24	D7	24	D18
25	E7	25	E18
26	A6	26	A17
27	B6	27	B17
28	C6	28	C17
29	D6	29	D17
30	E6	30	E17
31	A5	31	A16
32	B5	32	B16
33	C5	33	C16
34	D5	34	D16
35	E5	35	E16
36	A4	36	A15
37	B4	37	B15
38	C4	38	C15
39	D4	39	D15
40	E4	40	E15
41	A3	41	A14
42	B3	42	B14
43	C3	43	C14
44	D3	44	D14
45	E3	45	E14
46	A2	46	A13
47	B2	47	B13
48	C2	48	C13
49	D2	49	D13
50	E2	50	E13

FIGURE 12 CPCI J5 PIN ASSIGNMENT

Additional J4 / J5 pins

J4:
Row F = Ground
A1, B1, C1, A15, B15, C15 = Fused 3.3V
D1, E1, D15, E15 = Fused 5V

J5:
Row F = Ground
A1, B1, C1, A12, B12, C12 = Fused 3.3V
D1, E1, D12, E12 = Fused 5V

The fused power is to allow for active user circuits on a rear panel expansion card. A total of 2A per voltage can be used by the expansion card.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The cPCI4IP is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amps per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP Module can be secured against the carrier with the connectors. If more security against vibration is required then IP mounting kit can be used to attach the IP to the carrier. Dynamic Engineering has mounting kits available if your IP did not come with one.
http://www.dyneng.com/IPHardware.html

MTBF

The cPCI4IP has been modeled with Belcore reliability prediction software. The MTBF is reported as greater than1,290,549Hrs. GB 25C. [cPCI2IP value. CPCI4IP is TBD and estimated to be similar to the cPCI2IP]

Thermal Considerations

The cPCI4IP design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. The installed IP Modules may require forced air cooling. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite 3
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Logic Interfaces:	IP Logic Interface, PCI Interface -33 MHz. 32 bit, universal signaling
Access types:	IO, ID, MEM(64K), INT IP Spaces supported via cPCI bus accesses
CLK rates supported:	8 MHz or 32 MHz slot by slot selectable 33 MHz. cPCI
Software Interface:	Control Registers, and Installed IP. Programming procedure documented in this manual
Access Modes:	LW, Word or Byte to IP registers LW can be converted to two word accesses or as a LW to a 32 bit IP. LW to Internal PCI Interface Control registers. Bus error detection and handling.
Access Time:	Typical access time with 32 MHz. IP and double access mode is 500 nS.
Interrupt:	2 Interrupts per IP slot with separate enables., Programmable Bus error interrupt
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface:	50 pin Header Connectors
Dimensions:	6U 4HP
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Power:	RF filtered and fused to each IP slot. Re-settable “self healing” fuses.
User	8 position software readable switch 8 software controllable LED's
Other LED	LED's (3) on slot C power (±12,5) LED’s (4) used to show IP acknowledge to access – 1 per slot.
Slots	4 single wide IP slots with double wide and 32 bit capability in slot pairs A/B C/D
Temperature Range	0-70C Standard, -40 +85 available
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across Carrier
MTBF	Estimated 1.2 M Hrs. GB 25C

Order Information

Standard temperature range 0-70°C

cPCI4IP-MM	http://www.dyneng.com/cPCI4IP.html 6U cPCI card with 4 IP positions, front panel IO only
cPCI4IP-MM-RP	http://www.dyneng.com/cPCI4IP.html 6U cPCI card with 4 IP positions, J4/J5 IO only
cPCI4IP-MM-IO	http://www.dyneng.com/cPCI4IP.html 6U cPCI card with 4 IP positions, front panel IO and J4/J5 IO

Extended temperature range -40 - 85°C

cPCI4IP-MM-ET	http://www.dyneng.com/cPCI4IP.html 6U cPCI card with 4 IP positions, front panel IO only
cPCI4IP-MM-ET-RP	http://www.dyneng.com/cPCI4IP.html 6U cPCI card with 4 IP positions, J4/J5 IO only
cPCI4IP-MM-ET-IO	http://www.dyneng.com/cPCI4IP.html 6U cPCI card with 4 IP positions, front panel IO and J4/J5 IO
cPCI4IP-ENG	Engineering Kit for the cPCI4IP Software, Schematic, Debugging tools. There are several kits available. Please see the details on the website.
IP-DEBUG-BUS	http://www.dyneng.com/ipdbgbus.html IP test points, reset switch, fused power, quick switch isolated interface lines to allow hot swapping of IP cards.
IP-DEBUG-IO	http://www.dyneng.com/ipdbgio.html Isolate the IO connector to help with debugging. 50-pin header for system cable connection. 50 testpoints suitable for wire-wrap to allow loop-back connections. Locations for power and user circuits.
HDRterm50	http://www.dyneng.com/HDRterm50.html 50-pin header to 50 screw terminal converter with DIN rail mounting.

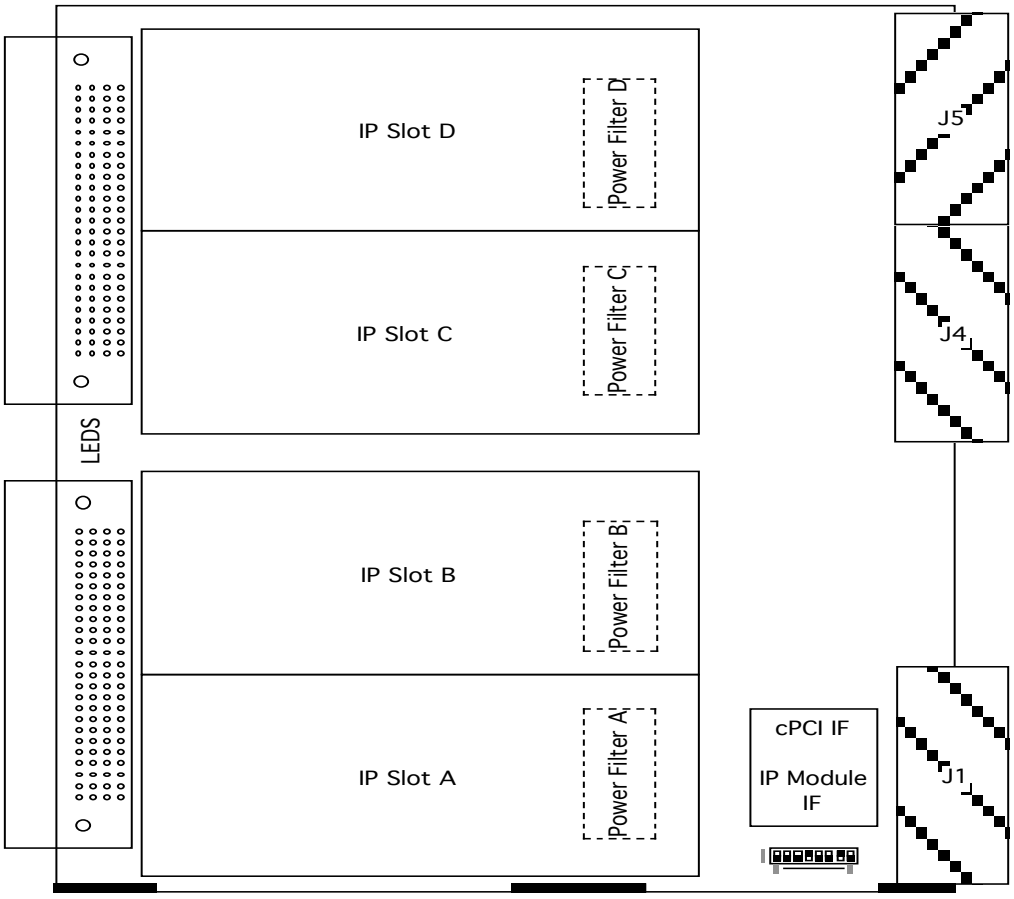
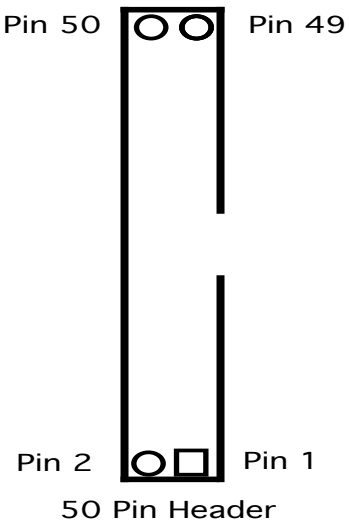


FIGURE 13 CPCI4IP CONNECTOR REFERENCE

The cPCI4IP has 4 slots (A,B,C,D) and 4 header connectors associated with those slots. Dual header connectors with ejectors and keying are used. A, B, C, D are marked on the bezel.

The wiring is 1:1 from the IP IO connector to the cPCI2IP header connector. The connectors are numbered to match standard ribbon cable as shown in the figure to the right.

The J4/J5 connector can be installed for Rear Panel IO. The IO is isolated with series 0Ω resistors [not installed] when J4/J5 are not installed.



50 Pin Header