DYNAMIC ENGINEERING
150 DuBois St. Suite C, Santa Cruz CA 95060
831-457-8891 **Fax** 831-457-4793
sales@dyneng.com
www.dyneng.com
Est. 1988

User Manual

PMC-BiSerial-S311

Bi-directional Serial Data Interface PMC Module

Revision B
Corresponding Hardware: Revision 1
10-2000-0101

PMC-BiSerial-S311
Bi-directional Serial Data Interface
PMC Module

Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz CA 95060
831- 457-8891
831-457-4793 FAX

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Manual Revision B1. 6/7/18.

Table of Contents

List of Figures

Product Description

PMC-BiSerial is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-BiSerial is capable of providing multiple serial protocols.

Please note: PMC-BiSerial-S311 has been updated to have two channels and reside on the newer BiSerial platform: PMC-BiSerial-VI-S311. It is recommended to purchase the new enhanced version.

Custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application. Several clocking options are available with the standard –IO version. The PMC Clock, 10 MHz. oscillator and external reference input are the clock sources. The source can be selected with software as can the divisor. A 12-bit counter is provided with a programmable divisor to offer a multitude of frequency options based on the three standard references. If a specific frequency is required that is not attainable with the standard choices we can install a “user” oscillator. Please be sure to select the proper source and clock divisors after reset to insure proper operation. Refer to the programming section for details.

Differential I/O is available on the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 130Ω. The resistors are in discrete 1206 packages to allow individual termination options for custom formats and protocols. There are 20 transceivers for the IO. The transceivers are programmable to allow more outputs or more inputs as needed for a specific protocol implementation.

The configuration implemented in the S311 uses four outputs for Tx data, Tx burst-clock Tx request, and Rx ready; and four inputs for Rx data, Rx burst-clock, Rx request, and Tx ready. The terminations on the inputs are programmable to be active or not.

All configuration registers support read and write operations for maximum software convenience. All addresses are long word aligned.

The PMC-BISERIAL conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

PMC-BiSerial uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors [height] to mate with the PMC-BiSerial, please let us know. We may be able to do a special build with a different height connector to compensate.

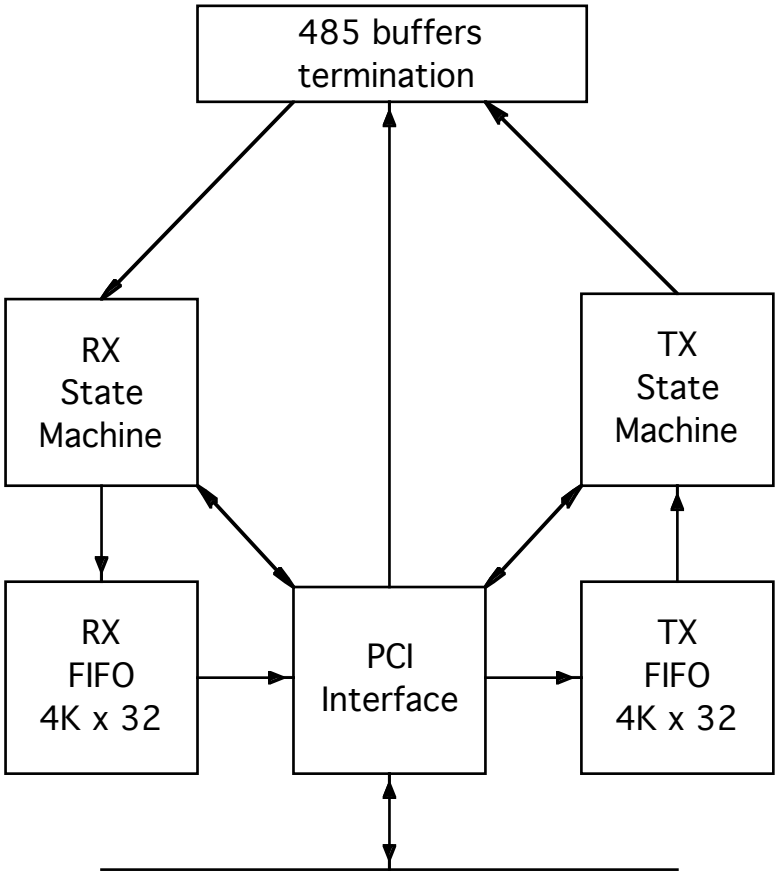

FIGURE 1 PMC-BISERIAL BLOCK DIAGRAM

The PMC-BiSerial-S311 implements the Northrop Grumman S-311 interface protocol. This protocol uses a burst clock to shift 18 bits of data. The data changes on the rising edge of the clock and is valid on the falling edge. The first bit is the sync bit, which is always high and the next 8 bits are the upper byte of the data shifted out MSB first. The next bit is the mode bit, which is zero for a data word and one for a command word. The final 8 bits are the lower byte of data shifted out MSB first.

Two additional signals are used in this protocol, request and ready. The request signal is asserted high by the transmitter at least two clock periods before the first clock. The request signal also remains asserted at least two clock periods after the falling edge of the last clock. After request goes low, at least four clock periods must elapse before it is reasserted.

The ready signal is asserted high by the receiver when it is ready to receive data i.e. it has been started and the Rx FIFO is not full. The ready signal can remain high between words as long as the receiver is able to receive data. No data should be transmitted unless ready is high, or does not exist.

The serial channels are each supported by a 4K by 32 bit FIFO (see figure1). The FIFO supports long word reads and writes. A path exists for loop-back testing of each FIFO. The PMC data path is 32 bits wide, while the data path from the FIFO to the Xilinx is 8 bits wide. The hardware automatically performs the 4 data accesses and byte lane manipulation to make the internal port appear as a 32-bit port to the PMC bus. The design is optimized for the system configuration with minimal delay on the PCI write to TX FIFO path and PCI read from the RX FIFO path. The added delay for reading and writing to the internal FIFO ports only affects the loop-back test path.

As the serial receive channel receives data, MSB first, it is stored in 18-bit words with the sync bit in the MSB (bit 17), the mode bit repositioned to bit 16 and the 16 data bits stored in bit 15 down to 0. The host can poll the empty flag status or use the programmable FIFO Almost Full flag to determine when data is available. The message can be read directly from the input FIFO.

The Output channel has a separate 4K x 32 FIFO. The FIFO is written as long words with the sync bit in bit position 17, the mode bit in bit position 16 and the 16 data bits in bit positions 15 to 0. Data is sent MSB first with the sync bit first followed by eight data bits, the mode bit, and the final eight data bits. Data is sent whenever the transmitter is enabled and data is stored within the FIFO and the ready signal is asserted from the receiver. Transmission completes and the transmitter is disabled when the FIFO becomes empty.

Interrupts are supported by the PMC-BISERIAL. For the S311 version, interrupts can be generated by the following conditions: transmission complete; transmitter almost empty; receiver almost full; receiver overflow; and a receiver interrupt, which can be configured to respond to any word received, or for a word received with a specific mode bit value, either zero or one.

The interrupts are individually maskable and a master interrupt enable is also provided as well as a force interrupt bit for testing purposes. The interrupt occurs on INTA. The FIFO levels and other status are also available for operating in a polled mode, if desired.

Theory of Operation

The PMC-BISERIAL is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design. In standard configuration, the PMC-BiSerial is a Type 1 mechanical with no components on the back of the board and one slot wide, with 10 mm inter-board height.

The PMC-BISERIAL-S311 is designed for transferring data from one point to another with a specific serial protocol. It features a Xilinx FPGA, which contains all of the registers and protocol controlling elements of the BISERIAL design. Only the transceivers, switches, and FIFOs are external to the Xilinx device.

A logic block within the Xilinx controls the PCI interface to the host CPU. The BISERIAL design requires one wait state for read or write cycles to any address other than the loop-back ports, which require eight. The wait states refer to the number of clocks after the PCI core decode and before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate with data state into the TRDY signal.

The PMC-BISERIAL-S311 is designed to transmit and receive data using the Northrop Grumman S-311 protocol. This protocol uses and 18 bit word to transfer 16 data bits and a mode bit indicating whether the word is data or command. In addition a sync bit, which is always high is sent as the first bit of a serial transfer. The data is written and read over the PCI bus with the sync bit as bit 17 of a 32-bit word, the mode bit as bit 16 and the 16 data bits occupying bit positions 15 through 0. However, when the bits are sent serially the sync bit is sent first followed by data bit 15 down to 8, next the mode bit is sent followed by data bits 7 down to 0. The bus clock speed can be anything from 0 to 1 MHz, but is nominally 250 kHz.

Clock reference sources include an on-board 10 MHz oscillator, the PCI clock and a user input clock. The reference clock is available at the base rate or after a programmable 12-bit divider. Please refer to the memory map for more details.

An interrupt can be generated by five conditions: transmit complete, determined by the transmit FIFO going empty; the transmit FIFO programmable almost empty; the receive FIFO almost full; receiver overflow, which occurs when an attempt is made to write to a full FIFO; and an additional receive interrupt, which can be configured to respond to any word received, or only words with mode bit zero, or only words with mode bit one. These conditions are latched until cleared by writing a one to the corresponding bit of the interrupt status register. Each interrupt is individually maskable by bits in the transmit and receive control

registers and there is also a master interrupt enable in the base control register.

The receiver can also be configured to selectively store only words with mode bit equal to one or only words with mode bit equal to zero.

The values used for the almost empty and almost full FIFO flags default to seven words from the empty and full conditions. However, resetting the FIFOs with the load bit held low allows these defaults to be changed. After the reset bit is set high again, writing to the FIFO writes to four registers in a continuously rotating order: almost empty lower eight bits, almost empty upper four bits, almost full lower eight bits, and almost full upper four bits. In order to write to the receive FIFO the test mode bit must be set to select the PCI bus as the data source. The flags are read from the FIFO that stores bits 31-24, therefore the values written to the level registers must be placed on this byte lane e.g. 0x10000000 translates to a value of ten hex or sixteen decimal. After the four registers are written the load bit is set high and the FIFO is ready for normal operation.

Address Map

Function		Offset	function	Type
bis_base	EQU	$00	base control register	read/write
bis_tx	EQU	$04	transmit base control	read/write
bis_rx	EQU	$0C	receive base control	read/write
bis_stat0	EQU	$14	status register 0	read/write
bis_stat1	EQU	$18	status register 1	read/write
bis_fifotx	EQU	$20	transmit FIFO access	read/write
bis_fiforx	EQU	$24	receive FIFO access	read/write
bis_dir_term	EQU	$28	direction & termination	read/write
bis_switch	EQU	$44	receive FIFO access	read

FIGURE 2 PMC-BISERIAL-S311 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the PMC-BiSerial. The addresses are all offsets from a base address. The carrier board that the PMC is installed into provides the base address.

The VendorId = 0x10EE. The CardId = 0x000F. Current revision = 0x02

Programming

Programming the PMC-BISERIAL requires only the ability to read and write data from the host. The PMC Carrier board determines the base address. This documentation refers to the first user address for the slot that the PMC is installed in as the base address.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to receive data the software is only required to enable the Rx state machine. If desired, data filtering can be configured and interrupts can be enabled. Data will be loaded into the FIFOs as it is received, as long as there is room.

If interrupts are to be used, the interrupt service routine should be loaded and the mask bits should be set. After the interrupt is received, appropriate action can be taken. New messages can be received even as the current one is read from the FIFO and data can be loaded into the Tx FIFO while data is being sent.

The end of transmission interrupt will indicate to the software that the Tx message has been started and that the message has terminated. If more than one interrupt has been enabled, then the SW needs to read the interrupt status register to see which source caused the interrupt. The interrupt status can be cleared by writing a one to the corresponding bit, then the interrupts can be re-enabled.

Before transmitting data, the FIFOs are enabled and the data loaded. If the clock rate desired is something other than the default rate then the rate should be selected. Be sure to set the clock source and rate bits appropriately. Once the complete message is loaded and the controls set properly the start bit can be set to cause the transfer to begin. If a slow clock rate is selected and a long message is sent then data can be loaded during transmission to save operational time. Care must be taken to insure that the FIFOs do not become empty prematurely, or the transmission will terminate. When the Tx interrupt is received the transmission has been completed and another message can be loaded. All that needs to happen for a second message to be sent is to load the FIFO and set the start bit.

To operate in a polled mode, read the Status 0 register during the transfer and take appropriate action when the full, empty or programmable flag shows that there is data to read or space to write. The PAE flag is implemented to provide an almost empty interrupt to allow the TX side to operate in an interrupt driven mode with longer messages. Similarly the PAF can be used to provide an almost full interrupt for the receive side to allow interrupt driven long message capability.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

Register Definitions

bis_base

$00 BISERIAL Control Register Port read/write

CONTROL BASE

DATA BIT	DESCRIPTION
31-23	spare
22	FRX_LD
21	FTX_LD
20	FIFO_EN
19-18	spare
17	INT_SET
16	INT_EN_MASTER
15	spare
14-13	clock pre-selector
12	clock post-selector
11-0	clock divisor

FIGURE 3 PMC-BISERIAL-S311 BASE CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or a reset command.

FRX_LD is tied to the RX FIFO WE2/_LD pin. FTX_LD is tied to the TX FIFO WE2/_LD pin. When the FIFOs are taken out of reset it is possible to set-up the FIFO to accept commands to program the level at which the programmable almost empty and programmable almost full signals operate. ***In the standard transfer mode these pins are set hi before FIFO_EN is set to use as a second WE control pin***. If the PAE and PAF flags are used then the FIFOs may require programming. See the theory of operation section for information on performing this operation.

FIFO_EN when ‘1’ takes the FIFO out of reset. To create a reset be sure to leave in the ‘0’ state long enough for the reference clock to capture the reset. This can be an issue if a slow transmission rate is chosen. To guarantee reset, the PCI clock should be used as a reference for both the Tx and Rx FIFOs temporarily then set back to the original settings.

INT_SET is used for test and software development purposes to create an interrupt request: 1 = assert interrupt request. 0 = normal operation. This is useful to stimulate interrupt acknowledge routines for development.

INT_EN_MASTER when ‘1’ gates all interrupts through to the PCI host. When ‘0’ the interrupts can be used for status without interrupting the host.

Clock Pre-Selector

00	oscillator
01	oscillator
10	external
11	PCI clock

The clock pre-selector is used to select which reference clock to use with the divisor hardware (the clock source). The external clock is on IO channel 0.

Divisor [11-0] is the clock divisor select bits. A counter divides the clock source. The reference clock for the counter is selected with the CLK Pre-Selector. The output frequency is [reference / [2(n+1)], n $\geq$ 1. The reference oscillator is 10 MHz in frequency. The counter divides by n+1 due to counting from 0 to n before rolling over. The output is then divided by two to produce a square wave output.

Post Selector when '1' sets clock out to clock divided, when '0', clock out is set to the reference clock specified by the pre-selector.

Please note that the 485 buffers are only rated for 12 MHz. With most systems the larger divisors will be used. The smaller divisors are provided for use with external oscillators and the external clock line.

bis_tx

$04 BISERIAL TX Control Register Port read/write

CONTROL TX	
DATA BIT	**DESCRIPTION**
31-4	spare
3	ignore_rdy
2	int_en_pae
1	int_en_tx
0	start_tx

FIGURE 4 PMC-BISERIAL-S311 TX CONTROL REGISTER BIT MAP

IGNORE_RDY when ‘1’ tells the transmitter to disregard the ready signal when sending data. This allows transmitter operation when the receiver does not supply a ready output. When ‘0’ (default) the ready is required to be asserted high for transmission to occur.

INT_EN_TX when ‘1’ enables the Tx interrupt. The default state is off. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the transmission is complete.

INT_EN_PAE when ‘1’ enables the FIFO Programmable Almost Empty interrupt. The default state is off. When enabled and the master interrupt enable is also enabled an interrupt is generated when the data level falls to the programmed level.

START_TX when ‘1’ will start a transmission assuming that there is data in the Tx FIFO. This bit is auto-cleared when the transmission is complete.

bis_rx

$0C BISERIAL RX Control Register Port read/write

CONTROL RX	
DATA BIT	**DESCRIPTION**
31-8	spare
7	testmode
6	filter_def
5	filter_int_en
4	filter_en
3	int_en_ovfl
2	int_en_paf
1	rx_int_en
0	start_rx

FIGURE 5 PMC-BISERIAL-S311 RX CONTROL REGISTER BIT MAP

Testmode when ‘1’ selects the PCI bus as the data source for Rx FIFO writes. Normally set to ‘0’ (default). Set to ‘1’ for FIFO loop-back or programming the almost full flag level.

Filter_def defines what mode bit value satisfies the filter test. When ‘1’, words with mode bit = ‘1’ satisfy the test, when ‘0’ (default), words with mode bit = ‘0’ satisfy the test.

Filter_int_en when ‘1’ enables the filter interrupt when the appropriate mode bit is seen (default disabled). The rx_int bit must also be set to generate an interrupt.

Filter_ en when ‘1’ enables data filtering. Only words with the appropriate mode bit value will be stored (default disabled).

Int_en_ovfl when ‘1’ enables the overflow interrupt (default disabled). The interrupt is asserted when an attempt is made to write to a full FIFO. It requires the master interrupt enable to be asserted to create a system level interrupt.

Int_en_paf when ‘1’ enables the RX FIFO Programmable Almost Full flag interrupt (default disabled). The interrupt becomes active when the data in the RX FIFO reaches a user programmed point of almost full. It requires the master enable to be asserted to create a system level interrupt.

Rx_int_en when ‘1’ enables the Rx interrupt to be active (default disabled). If filter_int_en is ‘0’, any word received will cause an interrupt, but if filter_int_en is ‘1’, only words whose mode bit matches filter_def will cause an interrupt.

Start_rx is a master enable required to be ‘1’ for the receive state machine to receive messages (default ‘0’).

bis_stat0

$14 BISERIAL Status Port [read only]

Data Bit	Status	
15	int_request	1 = interrupt request after int_en mask
12	fae_int	1 = tx almost empty interrupt condition has been met
11	tx_int	1 = transmit interrupt condition has been met
10	ftx_ffn	1 = tx fifo full, 0 = not full
9	ftx_faen	1 = almost empty, 0 = not almost empty
8	ftx_mtn	1 = tx fifo empty, 0 = not empty
7,6	spare	
5	rx_ovfl_int	1 = receive overflow condition has been met
4	faf_int	1 = rx almost full interrupt condition has been met
3	rx_int	1 = receive interrupt condition has been met
2	frx_ffn	1 = rx fifo full, 0 = not full
1	frx_fafn	1 = almost full, 0 = not almost full
0	frx_mtn	1 = rx fifo empty, 0 = not empty

FIGURE 6 PMC-BISERIAL-S311 STATUS REG 0 BIT MAP

Int_request when ‘1’ indicates that at least one of the maskable interrupts is active and enabled.

Fae_int when ‘1’ indicates that the Tx FIFO went from not almost empty to almost empty.

Tx_int when ‘1’ indicates that the transmit state machine was started and finished sending a message.

Rx_ovfl_int when ‘1’ indicates that an attempt was made to write data to a full Rx FIFO.

Faf_int when ‘1’ indicates that the Rx FIFO went from not almost full to almost full.

Rx_int when ‘1’ indicates that a word was received with the appropriate mode bit (as defined by filter_def). If filter_en is ‘0’ then any word received will cause this bit to be asserted.

The FIFO flags are active high. When the empty bit is high, then the FIFO is empty. When the empty flag is low, then the FIFO has at least one piece of data stored. When the Full Flag is set high, the FIFO is full. When not set, then the FIFO still has room.

bis_stat0

$14 BISERIAL Status Port [write only]

Data Bit	Function	
4	rx_ovfl_int_clr	1 = receive overflow condition cleared
3	rx_int_clr	1 = receive interrupt condition cleared
2	tx_int_clr	1 = transmit interrupt condition cleared
1	faf_int_clr	1 = rx almost full interrupt condition cleared
0	fae_int_clr	1 = tx almost empty interrupt condition cleared

FIGURE 7 PMC-BISERIAL-S311 STATUS REG 0 CLEAR BIT MAP

The interrupt condition bits in the Stat0 register are latched until explicitly cleared. The above bits, when set to '1' when a write is performed to this register, will clear the corresponding interrupt condition.

bis_stat1

[$18] BISERIAL Status Port [read/write]

Data Bit	Status
15-0	received word count

FIGURE 8 PMC-BISERIAL-S311 STATUS REG 1 BIT MAP

WORD_CNT 15..0 is the cumulative number of words received. The count is updated as each word is stored in the receive FIFO. The count is cleared when the receiver is disabled or when a write is performed to this register address (write data value is irrelevant). Even after the count has been cleared, the old count will be returned when this register is read until a new word is received, beginning a new count.

bis_fifotx

$20 BISERIAL TX FIFO read/write port

The BISERIAL supports 32-bit writes to the transmit data FIFOs although only 18 bits are actually transmitted with the S-311 protocol. Data is aligned D31-0. Normally this port is only written to. For loop-back testing the contents of the FIFO can be read from the “Xilinx” side of the FIFO. The reference clock must be set to the PCI source for the loop-back to work. The engineering kit contains software, which performs a TX FIFO loop-back. Once data is read from the FIFO it is no longer available for transmission.

bis_fiforx

$24 BISERIAL RX FIFO read/write port

The BISERIAL supports 32-bit reads from the receive data FIFOs although only 18 bits are received with the S-311 protocol. Data is aligned D31-0. Normally this port is only read from. For loop-back testing the contents of the FIFO can be written through the “Xilinx” side of the FIFO. The testmode bit must be set to cause the PCI bus to be selected as the data source. The engineering kit contains software, which performs an Rx FIFO loop-back.

bis_dir_term

$28 BISERIAL direction and termination Port [read/write]

CONTROL REGISTER DIR_TERM

DATA BIT	DESCRIPTION		
8-0	DIRection	10-0	0 = read, 1 = drive
23-16	TERMination	10-0	1 = terminated

FIGURE 9 PMC-BISERIAL-S311 DIRECTION TERMINATION CONTROL BIT MAP

The direction for each of the 20 differential pairs is controlled through this port. The port defaults to ‘0’ which corresponds to tri-stating the drivers.

Pull-up and Pull-down resistors built into some '485 interface devices may make the signal appear to be driven [if open] when in the tri-stated mode. Enabling the termination on a tristated line will yield approximately 2.5V on each side of the tri-stated driver.

The PMC-BISERIAL-S311 design sets the direction of the signals to be set to output except for the signal group IO 12-15 and IO 0, which are inputs. The table is shown for future use when we plan to add in a read/write parallel port on the unused transmission lines. Currently the forced bits are read-write but have no effect.

CONTROL	CORRESPONDING IO BIT(S)
DIR_0..3	IO_0..3.
DIR4	IO_4..7
DIR5	IO_8..11
DIR6	IO_12..15
DIR7	IO_16..19

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others, it will make sense to use the onboard terminations.

The terminations for the receive groups should be set to terminate with the user software in most cases. [term0 and term6]

CONTROL	CORRESPONDING IO BIT(S)
TERM_0..3	IO_0..3.
TERM4	IO_4..7
TERM5	IO_8..11
TERM6	IO_12..15
TERM7	IO_16..19

bis_switch
$44 BiSerial Switch Read Port read only

SWITCH READ PORT	
DATA BIT	**DESCRIPTION**
5	UB5
4	UB4
3	UB3
2	UB2
1	UB1
0	UB0

FIGURE 10 PMC-BISERIAL SWITCH READ BIT MAP

The Switch Read Port has the user bits. The user bits are connected to 6 switch positions. The switches allow custom configurations to be defined by the user and for the software to “know” how to configure the read/write capabilities of each IO line. Please note that only the lower 6 bits of the switch are implemented [8 positions on switch]. The silk-screen is marked with the ‘0’ and ‘1’ definitions.

Interrupts

PMC-BISERIAL-S311 interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with a PMC-BiSerial interrupt the software must read the interrupt status to determine the cause(s) of the interrupt, clear the interrupt condition(s) and process accordingly.

The PMC-BISERIAL-S311 Tx state machine generates an interrupt request when a transmission is complete and the INTEN bit in the control register is set. The transmission is considered complete when the Tx start bit is cleared. The interrupt is mapped to INTA on the PMC connector. INTA may be mapped to a different interrupt in your system. For example in our NT systems it is mapped to interrupt B. The source of the interrupt is obtained by reading status register 0. The status remains valid until the status register is written with the appropriate bit.

The interrupt level seen by the CPU is determined by the rest of the system. The master interrupt can be disabled or enabled through the bis_base register. The individual enables for the various interrupt conditions are controllable through bis_tx and bis_rx.

The individual enables operate after the interrupt holding latch, which stores the status for the CPU. Once the interrupt request is set, the way to clear the request is to write the proper bit to the interrupt status/clear register, assuming the original cause is no longer in effect or disable the master interrupt enable. The master enable is a mask and can be used to disable the interrupt from reaching the CPU, but still leaves the internal interrupt request hardware active, which is useful for polled operation.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled and the Tx, and programmable level interrupts enabled as needed. When bis_stat0 shows an interrupt pending, the appropriate action can be taken, if any, to remove the interrupt condition. Then the appropriate bit is written to the interrupt status/clear register to clear the request.

If interrupt driven the normal sequence to service an interrupt is to disable the master interrupt enable, then read the interrupt status/clear register to determine the cause of the interrupt. If an almost full or empty interrupt has occurred, the appropriate FIFO is read or written and the appropriate bit is then written to the stat0 register, which will clear only that bit and insure that interrupt conditions will not be missed. The master interrupt enable is once again asserted and the system is ready to capture the next interrupt event.

Power on initialization will provide a cleared interrupt request and interrupts disabled.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires and external cable with the following pins connected.

Data+	7 - 22
Data-	41 - 56
Clk+	9 - 24
Clk-	43 - 58
Request+	11 - 21
Request-	45 - 55
Ready+	12 - 26
Ready -	46 - 60

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BiSerial-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V[unused]	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 11 PMC-BISERIAL PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BiSerial-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V[unused]		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 12 PMC-BISERIAL PN2 INTERFACE

BiSerial-S311 Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-BiSerial. Also, see the User Manual for your carrier board for more information. GND* is a plane which is tied to GND through a 1206 0Ω resistor. AC or open are options – contact Dynamic Engineering.

IO_0p [ref clk+]	IO_0m [ref clk-]	1	35
IO_1p	IO_1m	2	36
GND*	GND*	3	37
IO_2p	IO_2m	4	38
GND*	GND*	5	39
IO_3p	IO_3m	6	40
IO_4p [TX_DATA+]	IO_4m [TX_DATA-]	7	41
GND*	GND*	8	42
IO_5p [TX_CLK+]	IO_5m [TX_CLK-]	9	43
GND*	GND*	10	44
IO_6p [TX_REQUEST+]	IO_6m [TX_ REQUEST -]	11	45
IO_7p [RX_READY+]	IO_7m [RX_READY-]	12	46
GND*	GND*	13	47
IO_8p	IO_8m	14	48
GND*	GND*	15	49
IO_9p	IO_9m	16	50
IO_10p	IO_10m	17	51
GND*	GND*	18	52
IO_11p	IO_11m	19	53
GND*	GND*	20	54
IO_12p [RX_REQUEST+]	IO_12m [RX_ REQUEST -]	21	55
IO_13p [RX_DATA+]	IO_13m [RX_DATA-]	22	56
GND*	GND*	23	57
IO_14p [RX_CLK+]	IO_14m [RX_CLK-]	24	58
GND*	GND*	25	59
IO_15p [TX_READY+]	IO_15m[TX_READY-]	26	60
GND*	GND*	27	61
IO_16p	IO_16m	28	62
GND*	GND*	29	63
IO_17p	IO_17m	30	64
GND*	GND*	31	65
IO_18p	IO_18m	32	66
GND*	GND*	33	67
IO_19p	IO_19m	34	68

FIGURE 13 PMC-BISERIAL FRONT PANEL INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC-BiSerial Module routed to Pn4. Also, see the User Manual for your carrier board for more information.

IO_0p	REFCLK+	IO_0m	REFCLK-	1	2
IO_1p		IO_1m		3	4
IO_2p		IO_2m		5	6
IO_3p		IO_3m		8	9
IO_4p	TX_DATAp	IO_4m	TX_DATAm	9	10
IO_5p	TX_CLKp	IO_5m	TX_CLKm	11	12
IO_6p	TX_REQUESTp	IO_6m	TX_REQUESTm	13	14
IO_7p	RX_READYp	IO_7m	RX_READYm	15	16
IO_8p		IO_8m		17	18
IO_9p		IO_9m		19	20
IO_10p		IO_10m		21	22
IO_11p		IO_11m		23	24
IO_12p	RX_REQUESTp	IO_12m	RX_REQUESTm	25	26
IO_13p	RX_DATAp	IO_13m	RX_DATAm	27	28
IO_14p	RX_CLKp	IO_14m	RX_CLKm	29	30
IO_15p	TX_READYp	IO_15m	TX_READYm	31	32
IO_16p		IO_16m		33	34
IO_17p		IO_17m		35	36
IO_18p		IO_18m		37	38
IO_19p		IO_19m		39	40
				41	42
				43	44
				45	46
				47	48
				49	50
				51	52
				53	54
				55	56
				57	58
				59	60
				61	62
				63	64

FIGURE 14 PMC-BISERIAL-S311 PN4 INTERFACE

Applications Guide

Interfacing

The pinout tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC-BiSerial when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. PMC-BISERIAL does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the BiSerial pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68 screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68
[http://www.dyneng.com/HDEterm68.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BiSerial is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BISERIAL design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering’s products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options. http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Host Interface:	PCI Mezzanine Card
Serial Interface:	RS-485 Tx_Data, Tx_Clk, Tx_Request, Rx_Ready, Rx_Data, Rx_Clk, Rx_Request, Tx_Ready, REFCLK
TX CLK rates generated:	12 bit divisor with 10 MHz, 33 MHz. and REFCLK input rates. Other rates available with special oscillator installation
Software Interface:	Control Registers, Status Ports, FIFO
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses except FIFO loop-back, which require 8.
Interrupt:	Tx interrupt at end of transmission Programmable Almost Empty Programmable Almost Full Rx Overflow, Configurable Rx interrupt
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{O}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC-BISERIAL-IO-S311	PMC Module with 1 Tx and 1 Rx serial channels, Programmable data rates Special protocol support, RS-485 drivers and receivers 32 bit data interface
Eng Kit–PMC-BISERIAL-S311	HDEterm68 - 68 position screw terminal adapter HDEcabl68 - 68 IO twisted pair cable Technical Documentation, 1. PMC-BISERIAL Schematic 2. PMC-BISERIAL-S311 Reference test software 3. PMC-BISERIAL-S311 Win7 Driver Data sheet reprints are available from the manufacturer's web site reference software.

***Note**: The Engineering Kit is strongly recommended for first time* PMC-BISERIAL *buys.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.