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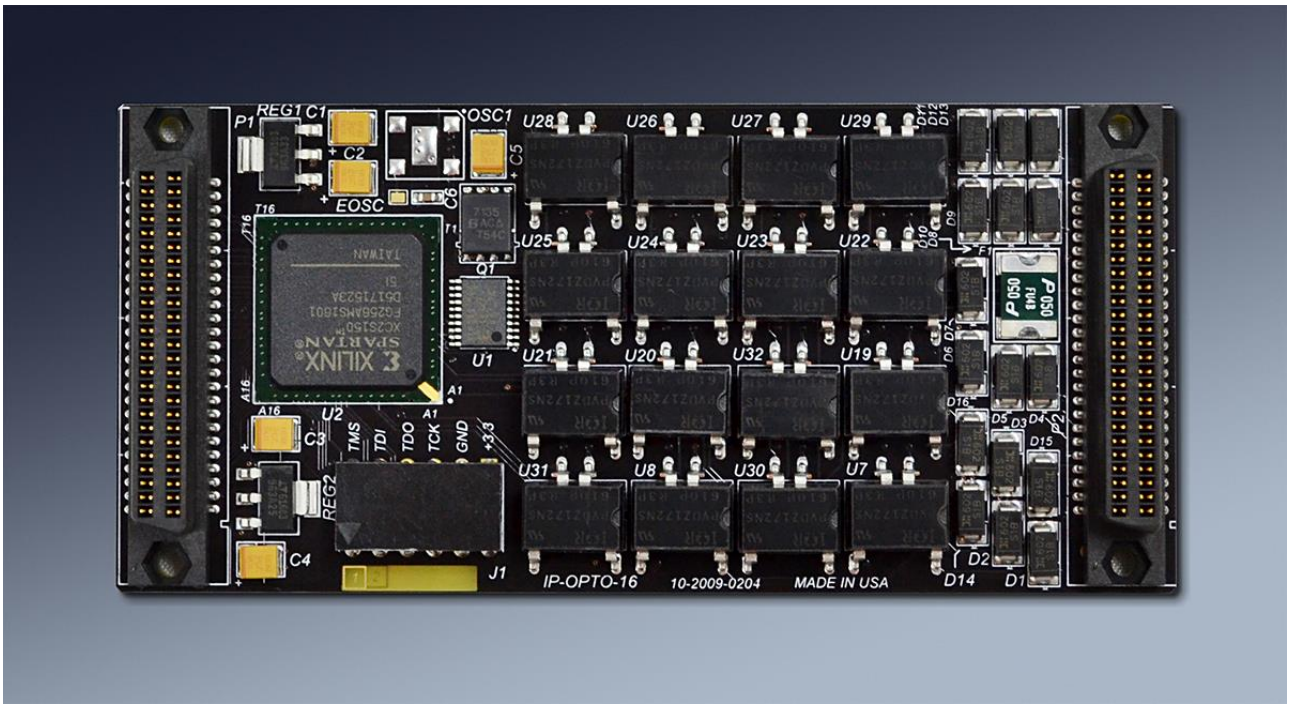
User Manual

IP-OptoISO-16

16 Channel Optically Isolated Drivers

IP Module



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IP-OptoISO-16
16 channel Serial Data Interface
IP Module

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised 9/14/16

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Product Description

IP-OptoISO-16 is part of the IP Module family of modular I/O components. The IP-OptoISO-16 is designed to provide optically isolated FET switches suitable for high and low side high voltage switching applications. The FETôs are rated for 60V and 1.5A DC. The traces on the IP-OptoISO-16 are designed to handle 1.5A+. The FETôs have low power dissipation even at full voltage and current. Each of the Outputs have a clamping DIODE for protection. The Diodes are rated for 100V and a peak of 30A.

With the Revision 04 fab the Xilinx has been upgraded to an Industrial Temperature Spartan II device. Additional space is available for new features, and Industrial Temperature is now standard.

Additional features include two counter timers. The counter timers provide periodic interrupts and can be used to create a square wave output. The square wave can be routed onto the outputs creating a high voltage clock.

The Xilinx has room for additional features or custom protocols. Please see our web page for current protocols offered. If you do not find it there we can redesign the state machines and create a custom interface protocol. That protocol will then be offered as a ñstandardòspecial order product. Please contact Dynamic Engineering with your custom application.

IP-OptoISO-16 supports 8 and 32 MHz IP Bus operation. The IP Clock is used or the reference clock for the counter-timers. Please be sure to set the appropriate clock selection after reset to insure proper operation. Please refer to the programming section for details.

The Opto Isolators are designed to reset to the off state ï FETôs in high impedance. The opto isolators have an LED on the IP side of the circuit. When sufficient current is passed through the LED the FET is enabled to the low impedance state. The current source for the LED is another FET which must be enabled [software] before any of the channels can operate. The Cathode side of the LED is connected to the Xilinx. The Xilinx circuit is implemented as an open-drain output so no current flows when the circuit is off. When one or more of the isolated outputs are programmed to be enabled, the Xilinx drives the cathode low allowing current to flow through the LED which turns on the FET. The current is controlled with a limiting resistor which has been selected for performance. With the optimal current selection the ñonòand ñoffòtimes for the FET can be minimized.

The IP-OptoISO-16 switching time will depend to a great extent on the system to which it is connected. Within the operational parameters, more current and less voltage will

result in faster times. Typical switching times of less than 250 uS are observed in our test fixture.

All configuration registers support read and write operations for maximum software convenience. Word and byte operations are supported (please refer to the memory map).

Frequently it is necessary to correlate the time and the event. The IP-OptoISO-16 design supports an enhanced MC68230 capability with two - 32 bit counter - timers. The counter-timers are easy to use with a minimum of registers to access and complete independence. The IP clock is used as a reference; both 8 and 32 MHz can be used.

Counter/Timer A features a 32 bit down-counter with a pre-load register. The counter output is tested against a "zero" value. When zero the counter is re-loaded with the pre-load value to create a cycle. At each zero detection an interrupt can be generated. At each zero detection a waveform can be transitioned. The waveform can be enabled onto the upper data bit.

Counter / Timer B has a 32 bit up counter which can be cleared by the software. The counter output is masked with a user programmable value to select a particular counter bit or bits to use for interrupt creation. The counter output is also available to read via software and can serve as a real-time clock.

The IP-OptoISO-16 conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Since the IP maintains plug and software compatibility while mounted on different form factors, system prototyping may be done on one IP Carrier board, with final system implementation done on a different one.

Theory of Operation

IP-OptoISO-16 features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the IP-OptoISO-16 design. Only the Opto Isolators and related circuitry are external to the Xilinx.

IP-OptoISO-16 is a part of the IP Module family of modular I/O products. It meets the IP Module Vita Standard. In standard configuration it is a Type II mechanical with low profile components on the back of the board and one slot wide. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

A logic block within the Xilinx device contains the decoding and timing elements required for the host CPU to interface with the IP bus. The timing is referenced to the 8 or 32 MHz IP logic clock. The IP responds to the ID, INT, MEM, and IO selects. The IP-OptoISO-16 design requires two wait states for read or write cycles to any IO address. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host removes the SEL line. Local timing terminates a write cycle prior to the SEL being de-asserted. If no hold cycles are requested by the host, IP-OptoISO-16 is capable of supporting 16+ MB per second data transfer rate with a 32 MHz reference rate.

Please remember that the IP can switch the controls faster than the output can change states. If IP-OptoISO-16 is commanded to change the state of an output at a rate faster than the transition time for your system then partial switching will result.

The OptoIsolator Drain and Source connections are brought out to the IP IO connector. The Drain will be connected to the source when enabled and isolated when disabled.

The Source side is diode protected ï referenced to the system ground. The optoisolators have internal diodes between the Source and Drain. If the Source voltage rises above the Drain voltage the internal protection diode will help to protect the device. The two diodes provide the optoisolators with protection against reverse loading from driving inductive loads etc.

For a High side switch the reference voltage should be connected to the D side side and the switched signal to the Source side. With an external pull-down the S side can be held low except when the optoisolator is enabled.

For a Low side switch the Source side can be grounded or tied to a lower voltage and the Drain side used to connect to the system. A pull-up to the higher reference voltage will hold the system at the upper voltage except when the optoisolator is enabled.

The Fused +5 and Digital ground can be used as the reference voltage and ground if desired. The Power and Ground connections are provided as a convenience for software development when the high voltage supply is not available and loss of the isolation capability can be overlooked. Be careful not to tie the digital ground to the SYS GND unless the grounds really are at the same potential. For development purposes with the SYS GND isolated it can be connected to the Digital Ground.

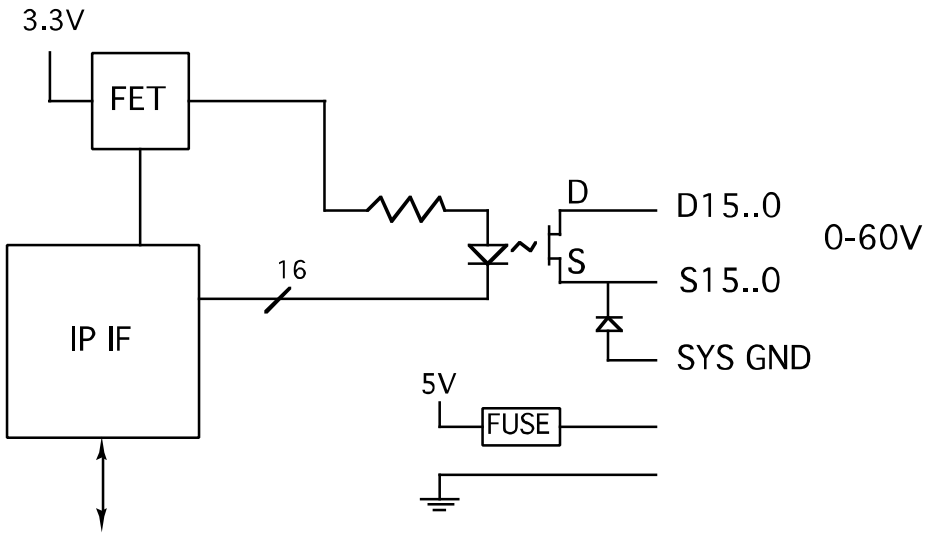


FIGURE 1 IP-OPTOISO-16 BLOCK DIAGRAM

The Counter Timer circuits can be used to control the pulse timing when your system requires a pulsed output. The counters can be programmed to provide interrupts on a periodic basis. One can be set-up for the width active and one for the frequency of the pulses. Interrupts can be generated with each occurrence to prompt the software to make the next state change for an output. Your operating system may provide reliable timer(s) that you can use instead.

If your system requires a periodic pulse with a 50% duty cycle [like a clock] then CTA can be used to generate the waveform without software intervention. The waveform can be muxed onto any of the OUT signals.

For ease of use the defintions for the OUT signals are done on a logical basis. The software controls are inverted before going to the Opto Isolators to provide a 1 = FET on situation. The control for the Opto Isolator LED power is also logically defined.

Counter B can be used as a real time clock. The Counter starts at ñ0ò and counts up based on the IP clock. The ñtimeò from start can be calculated based on the count and the period of the IP clock in use. The counter can be reset to start at a known point in time. The hold function allows the software to read the counter without risk of data from two different counts. While the hold bit is set the data is static for the host, and the counter continues to count in the back-ground.

Address Map

Function	Offset	Type
ip_optoiso_base	0x00000000	0 base control address
ip_optoiso_fet	0x00000002	1 FET OUT control
ip_optoiso_wav	0x00000004	2 FET OUT Mux control
	0x00000006	3 unused
ip_optoiso_stat	0x00000008	4 interrupt status
	0x0000000a	5 unused
	0x0000000c	6 unused
	0x0000000e	7 unused
	0x00000010	8 unused
ip_optoiso_tc	0x00000012	9 Timer Counter control
ip_optoiso_tdl	0x00000014	10 read timer data lower
ip_optoiso_tdu	0x00000016	11 read timer data upper
ip_optoiso_p_l	0x00000018	12 pre-load lower
ip_optoiso_p_u	0x0000001a	13 pre-load upper
ip_optoiso_tml	0x0000001c	14 timer mask lower
ip_optoiso_tmu	0x0000001e	15 timer mask upper
	0x00000020	16 unused
	0x00000022	17 unused
	0x00000024	18 unused
ip_optoiso_vect	0x00000026	19 vector register access

FIGURE 2 IP-OPTOISO-16 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-OptoISO-16. The addresses are all offsets from the IO space base address.

Programming

Programming IP-OptoISO-16 requires only the ability to read and write data in the host's I/O space. The IP Carrier board determines the base address of this address space. This documentation refers to the base address as the beginning of the I/O space for the slot in which the IP is installed.

In order to operate, the software is required to enable the FET LED power and then activate the FETôs as required. More complex programming can make use of the Counter/Timer and waveform generator to control the OUT signals.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example $40 is a valid user vector for the Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The IP-OptoISO-16 is an auto-vectored device with support for vectored interrupts to support installations that require an interrupt vector. The interrupt service routine should be loaded and the desired interrupts enabled. Interrupts can be generated when the counter/timer(s) complete(s).

SW needs to read the interrupt status register to determine the source(s) of the interrupt. to see which source caused the interrupt. In order to avoid missing an interrupt, the bits in this register must be explicitly cleared by writing the appropriate bit as a ó1ô It is a good idea to clear the status bits before the counter time is enabled to insure that the value read by the interrupt service routine came from the current operation.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

REGISTER DEFINITIONS

ip_optoiso_base

$00 OptoISO Control Register Port read/write

Base CONTROL REGISTER

DATA BIT	DESCRIPTION
15-6	spare
5	CTB Interrupt En
4	CTA Interrupt En
3	spare
2	Force Interrupt
1	Master Interrupt En
0	FET LED EN

FIGURE 3 IP-OPTOISO-16 CONTROL REGISTER 0 BIT MAP

0. FET LED EN when ó1ô enables the Opto Isolator LED Power. Default = ó0ô Must be enabled for OUT control bits to control the Outputs.

1. Master Interrupt En when ó1ô enables any of the programmed interrupts to cause an interrupt to the host when they become active.

2. Force Interrupt when ó1ô and the Master Interrupt Enable is enabled will cause an interrupt to the host. This function is used for test and software debugging.

4 CTA Interrupt En when ó1ô allows the Counter Timer A to cause an interrupt to the host. The Master Enable must be enabled. Status can still be read for polled operation.

Counter A is a 32 bit down counter. The counter is reloaded with the pre-load value in the when the counter returns to 0. [N+1] For example: with the IP clock set to 8 Mhz and the pre-load set to a 0x3d08ff value the programmed half period would be 4000000*125 = 500 mS between interrupts and a 1 second waveform period.

5 CTB Interrupt En when ó1ô allows the Counter Timer B to cause an interrupt to the host. The Master Enable must be enabled. Status can still be read for polled operation.

Counter/Timer B is a 32 bit up counter. The counter output is masked with the value in the mask register to pick off the period for the interrupt stream. For example: with the IP clock set to 8 Mhz and the mask set to a 0x00000040 the 7th bit would be selected for a divide by 64*2*125 = 16 uS period.

ip_optoiso_fet

$02 OptoISO Control Register Port read/write

DIRECTION CONTROL REGISTER	
DATA BIT	**DESCRIPTION**
15-0	Individual OUT control bits 15-0

FIGURE 4 IP-OPTOISO-16 FET REGISTER BIT MAP

Each OUTPUT channel has a bit corresponding to the FET control. When á1ô the individual FET is enabled and the OUT signal(s) will have the same potential as the reference voltage supplied. Please note that there will be a small voltage drop across the FET. Please refer to ip_optiso_wav.

ip_optoiso_wav

$04 OptoISO Control Register Port read/write

TERMINATION CONTROL REGISTER	
DATA BIT	**DESCRIPTION**
15-0	Individual mux control bits for OUT signals

FIGURE 5 IP-OPTOISO-16 OUTPUT MUX REGISTER BIT MAP

Each OUT signal has a mux to allow the output to be controlled from the ip_optiso_fet definition or the waveform output from CTA. The default is FET bitmapped control. Writing a á1ô to a bit will switch to CTA waveform control. Any number of bits can be set to bit mapped or waveform control. Please note that the waveform has a period 2x the programmed time. The waveform switches state at each interrupt occurrence.

ip_optoiso_stat

$08 OptoISO Control Register Port read/write

IO UPPER CONTROL REGISTER

DATA BIT	DESCRIPTION
15-12	Revision Major
11-8	Revision Minor
7-6	undefined
5	INT CTB masked
4	INT CTA masked
3	undefined
2	INT RQST
1	INT CTB unmasked
0	INT CTA unmasked

FIGURE 6 IP-OPTOISO-16 STATUS REGISTER BIT MAP

When the terminal conditions are met for CTA/CTB the hardware will output a pulse which is captured and held as the unmasked status. The bits are then masked and ored to create the interrupt request. If operating in polled mode the unmasked signals will be available even if the interrupts are not enabled.

The status bits are cleared by writing to the unmasked positions. Writing a 0x01 will clear the unmasked and masked INT CTA bits.

If the interrupts are enabled the status clear will remove the interupt request. The status clear should be part of the ISR.

Revision Major and Revision Minor fields are added
with the 1.2 = major.minor release. 9/14/16

ip_optoiso_tc

$0x12 OptoISO Control Register Port read/write

CONTROL REGISTER BASE	
DATA BIT	**DESCRIPTION**
15-6	spare
5	hold timerB 0 = disabled, 1 = hold
4	clear timerB 0 = run, 1 = clear
3-1	spare
0	timerA load 0 = run , 1 = load

FIGURE 7 IP-OPTOISO-16 TIMER CONTROL REGISTER BIT MAP

0. Counter/Timer A load when ó1ô loads the value in the pre-load register into the down counter. When ó0ô the counter decrements until the terminal count of ñ0ò is reached at which point the counter re-loads the pre-load value and repeats the cycle. The load bit is not needed because the counter will eventually roll over and reload anyway. If a large count was previously loaded or if the software wants to have a consistent period from a known point in time then the load bit should be used.

4. Clear Counter/Timer B when ó1ô forces the second counter timer to 0. This function is useful to restart the ñreal time clockò to a known value at a known time.

5. Hold Timer when ó1ô will stop the Counter/Timer B from updating the read-back register. Counter/Timer B will continue to run. The register will be stable allowing the two reads of the register data to happen without the stored count changing. ñ0ò= update the counter read-back register.

Pre-Load Registers

ip_optoiso_p_l $18 OptoISO Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	pre-load 15-0

FIGURE 8 IP-OPTOISO-16 PRE-LOAD LOWER BIT MAP

ip_optoiso_p_u $1A OptoISO Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	pre_load 31-16

FIGURE 9 IP-OPTOISO-16 PRE-LOAD UPPER BIT MAP

The pre-load registers are combined internally to form a 32 bit pre-load value to use with Counter/Timer A. Counter/Timer A is loaded with the value in the Pre-Load registers when the counter reaches zero. The counter can also be loaded with the software command via the TC register. The counter will count from the value down to zero creating an N+1 total count. The counter will re-load the value on the next count.

The Counter Timer A has the option of creating an interrupt at each zero crossing ï period N+1.The wave out option can also be enabled. The waveform is generated by switching each time the zero count is detected. A square wave is generated with a period of 2(N+1). The reference period is the IP clock which can be 125 nS or 31.25 nS depending on the carrier selection made.

Because of the architecture, the period selected with Counter/Timer A is arbitrary. Most OS/CPU can not handle interrupts faster than 10 uS. The counter output is registered and then checked against a count of 2 and re-registered. The count value checked is ò2ôto account for the double pipeline delay. The counter will be at ñ0òwhen the check reaches ñ2ò Because of the checking scheme the minimum count needs to be larger than ò2ôor the hardware will miss the first ñ2òand not see it until the counter rolls over. At 8 MHz. The roll over time is approximately 9 minutes.

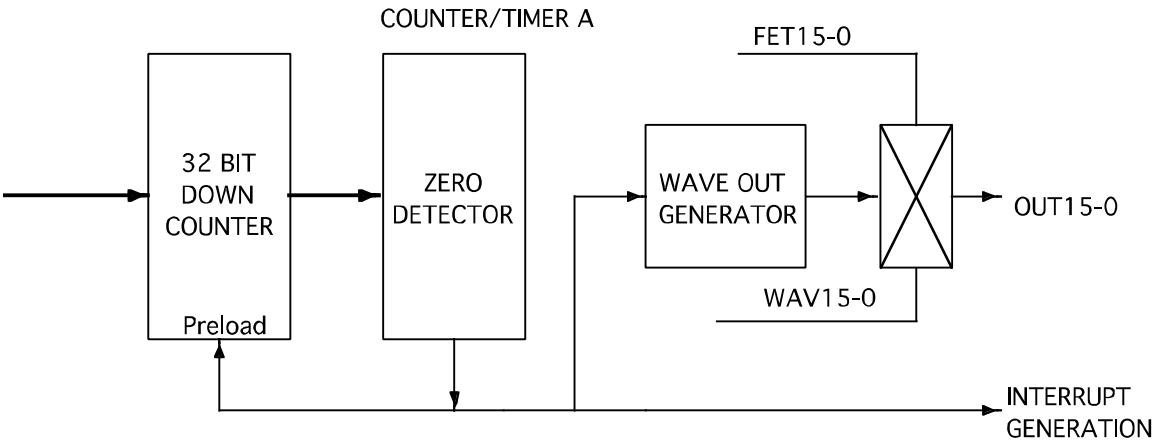


FIGURE 10 IP-OPTOISO-16 COUNTER/TIMER A

Mask Registers

ip_optoiso_tml 0x1C OptoISO Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	mask 15-0

FIGURE 11 IP-OPTOISO-16 MASK LOWER BIT MAP

ip_optoiso_tmu 0x1E OptoISO Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	mask 31-16

FIGURE 12 IP-OPTOISO-16 MASK UPPER BIT MAP

The mask registers are combined internally to form a 32 bit mask value to use with Counter/Timer B. Counter/Timer B is a 32 bit up counter which can be cleared to ô0ô The counter rolls over at the maximum count. Each counter bit is masked with the mask registers corresponding position. If the Mask(n) = ô1ôand the counter(n) is also a ô1ôthen the output will be ô1ô The output from the AND array is orôd to determine if any of the counter bit ï mask combinations are active. When a counter bit becomes active and the mask is set an interrupt is generated. The interrupt will be generated on the period of the counter selected with the mask. The counter uses the IP clock as a reference. The period selected is 2 * 2(n) * [125 or 31.25]. For example a 0x40 and 8 MHz reference rate would create a periodic interrupt with a period of 16 uS. [2*64*125 nS]

Read-Back Registers

ip_optoiso_tdl 0x14 OptoISO Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	read-back 15-0

FIGURE 13 IP-OPTOISO-16 READ-BACK LOWER BIT MAP

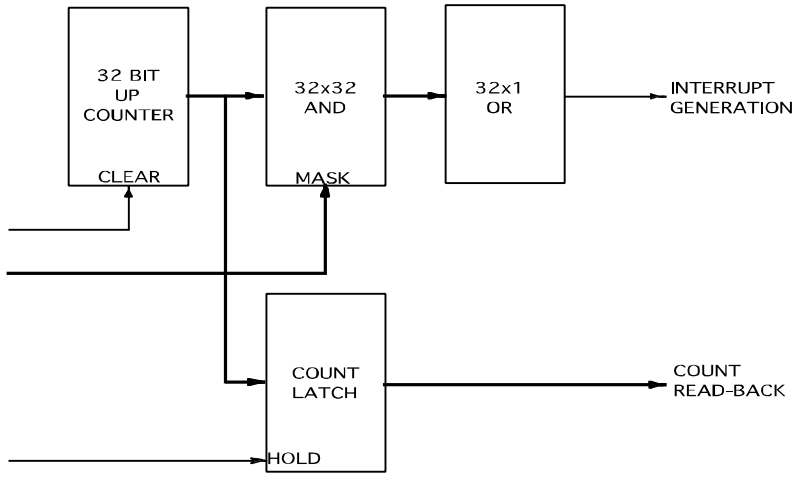
ip_optoiso_tdu 0x16 OptoISO Control Register Port read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	read-back 31-16

FIGURE 14 IP-OPTOISO-16 READ-BACK UPPER BIT MAP

Counter/TimerB has a read-back port for the count to be read by the host. The count is pipelined and stored into an output register. The register is updated unless the Hold [see tc register] bit is set. When the Hold bit is set the output register is disabled from updating; CTB continues to count. Two reads are needed to get the entire 32 bit word via the 16 bit IP data bus. If only one word is desired then the Hold bit can be ignored.

FIGURE 15 IP-OPTOISO-16 COUNTER/TIMER B



ip_optoiso_vect

$26 OptoISO Interrupt Vector Port read/write
The interrupt vector for the IP-OptoISO-16 is stored in this byte wide register. This read/write register is initialized to 0XFF upon power-on reset or software reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered.

INTERRUPTS

All IP Module interrupts are vectored. The vector from the IP-OptoISO-16 comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-OptoISO-16 Counter Timer Modules can generate interrupts. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector. The source of the interrupt is obtained by reading the interrupt status register. The status remains valid and the interrupt remains active until the status register bits are explicitly cleared.

The interrupt level seen by the CPU is determined by the IP Carrier board and bus being used. The master and individual interrupts can be disabled or enabled via the base register. The enables operate after the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to reset the board, clear the latched interrupt bit, or disable the interrupt. The Interrupt Status bits must be cleared before the interrupt is re-enabled or another interrupt will be generated.

Power on initialization will provide a cleared interrupt request, interrupts disabled, and interrupt vector of $FF.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-OptoISO-16 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-OptoISO-16-IO board will be recorded with a new code in the DRIVER ID location.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($09) OptoISO-16
0D	Revision	($A0)
0F	reserved	($00) Customer Number
11	Driver ID, low byte	($00) Design Number
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($26)

FIGURE 16 IP-OPTOISO-16 ID PROM

Loop-back

The Engineering kit has reference software, which includes an external LED Visual test. The test assumes the IP-Debug-IO is connected with the following modifications.

Jumper digital GND to reference GND
41 43

Tied Drains together and to Fused +5

34	2	10	18	26
35	4	12	20	28
36	6	14	22	30
37	8	16	24	32

Add LEDs to S0-15 with : S resistor A-LED-C GND as the topology
We used two bus wires to create a ground and soldered the resistor to the pad and the other end to the LED. The Cathode of the LED was then connected to the bus wire.

S0	1	200Ý	-|>|-	bus wire (gnd)
S1	3	200Ý	-|>|-	bus wire (gnd)
S2	5	200Ý	-|>|-	bus wire (gnd)
S3	7	200Ý	-|>|-	bus wire (gnd)
S4	9	200Ý	-|>|-	bus wire (gnd)
S5	11	200Ý	-|>|-	bus wire (gnd)
S6	13	200Ý	-|>|-	bus wire (gnd)
S7	15	200Ý	-|>|-	bus wire (gnd)
S8	17	200Ý	-|>|-	bus wire (gnd)
S9	19	200Ý	-|>|-	bus wire (gnd)
S10	21	200Ý	-|>|-	bus wire (gnd)
S11	23	200Ý	-|>|-	bus wire (gnd)
S12	25	200Ý	-|>|-	bus wire (gnd)
S13	27	200Ý	-|>|-	bus wire (gnd)
S14	29	200Ý	-|>|-	bus wire (gnd)
S15	31	200Ý	-|>|-	bus wire (gnd)

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-OptoISO-16. Pins marked n/c below are defined by the specification, but not used on the IP-OptoISO-16. Also see the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		n/c		5		30	
	D2		MEMSEL*		6		31
D3		n/c		7		32	
	D4		INTSEL*		8		33
D5		n/c		9		34	
	D6		IOSEL*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		INTREG0*		17		42	
	D14		A4		18		43
D15		n/c		19		44	
	BS0*		A5		20		45
BS1*		n/c		21		46	
	n/c		A6		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		GND		25		50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 17 IP-OPTOISO-16 LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-OPTOISO-16. Also see the User Manual for your carrier board for more information.

S0	D0	D12	S13	1	2	26	27
S1	D1	D13	S14	3	4	28	29
S2	D2	D14	S15	5	6	30	31
S3	D3	D15		7	8	32	33
S4	D4	FUSED+5V	FUSED+5V	9	10	34	35
S5	D5	FUSED+5V	FUSED+5V	11	12	36	37
S6	D6	DGND	DGND	13	14	38	39
S7	D7	DGND	DGND	15	16	40	41
S8	D8	USR_FREQ	GNDREF	17	18	42	43
S9	D9	GNDREF	GNDREF	19	20	44	45
S10	D10	GNDREF	GNDREF	21	22	46	47
S11	D11	GNDREF	GNDREF	23	24	48	49
S12		GNDREF		25		50	

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 18 IP-OPTOISO-16 IO INTERFACE

The Fused +5 has a current limit of 500 mA. The USR_FREQ is connected to the Xilinx and has a 1K pull-up. USR_FREQ is for custom requirements. GNDREF should be tied to the system ground. DGND is normally not connected.

On early revisions of this board the ñDòpins were tied together within the board. Revision C and later has the separated D side available to allow high, low side and mixed switching.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances or high currents. The IP-OptoISO-16 can handle currents much larger than ribbon cable or most carriers. With a pulsed system and an RMS current within specifications larger currents can be accommodated with standard ribbon cable and carriers.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. The Optically Isolated Outputs are designed to handle power supplies which do not come up together. The maximum ratings for the devices must be observed. 60V and 1.5A DC.

The rest of the IP-OptoISO-16 components must be treated as CMOS ï proper handling techniques must be observed. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within .7 volts of ground potential.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-OptoISO-16 is constructed out of 0.062 inch thick High Temperature FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat dissipation. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-OptoISO-16 design consists of CMOS and FET circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
Internet Address support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Parallel Interface	16 Optically Isolated Outputs. 0-60V, 1.5A High side & low side switch configurations supported.
Software Interface:	Control Registers, ID PROM, Vector Register, Status Ports, FIFOs two counter timers with waveform generator
Initialization:	Hardware Reset forces all registers to 0 except the Vector Register which resets to 0XFF.
Access Modes:	Word in IO Space (see memory map) Word in ID Space Vectored interrupt
Access Time:	back-to-back cycles in 500ns (8MHz.) or 125 nS (32 MHz.) to/from FIFO
Wait States:	1 to ID space, 2 to IO, MEM, or INT space
Interrupt:	CTA and CTB timer interrupts
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{o}C for uniform heat across IP
Power:	Typical 55 mA @ 5V

Order Information

IP-OptoISO-16	IP Module with 16 Optically Isolated Outputs 16 bit IP interface, 60V 1.5ADC per channel Extended Temperature Standard
-ROHS	Add this extension for ROHS compliant assembly. Standard leaded solder used otherwise
	http://www.dyneng.com/ip_optoiso_16.html
Tools for IP-OptoISO-16	IP-Debug-Bus - IP Bus interface extender http://www.dyneng.com/ipdbgbus.html
	IP--Debug-IO - IO connector breakout http://www.dyneng.com/ipdbgio.html
SW	Currently available SW is included with the purchase of IP-OptoISO-16. Please check the webpage for current offerings ï typically Win7, Linux, VxWorks.