



DYNAMIC ENGINEERING

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Est. 1988

Statement of Volatility PCIeBPMCX2

Manufacturer Part Number: PCIeBPMCX2, includes all options (-SCSI,-FAN1, etc.)

Manufacturer Part Description: PCIe carrier with 4 lanes, 2 PMC positions with 32/33 up to PCI-X, local power supplies and user features.

Memory Type: Bridge and EEPROM

Memory Size: Tundra [IDT] Tsi384: Internal registers for configuration, FIFO memory to support link traffic. FIFO on PCIe lanes includes Four, 128-byte read completion buffers. FIFO on PCI(x) bus is a 4K byte read completion buffer.

Optional EEPROM: normally **not installed**. Memory to provide additional default settings for the bridge device. Programmed via configuration space on host side, not directly user configurable.

Volatility: FIFO memory is continuously rewritten during operation and effectively cleared by this process. EEPROM is non-volatile when installed.

User Accessible: EEPROM can be used to store Bridge configuration values by the user. FIFO within Bridge is not user accessible in the traditional sense as the PCIe traffic is flowing through these memories without user control.

Clearing Procedure: Use and Power cycle for FIFO memory. To clear the EEPROM a standard 3 pass write cycle would be required. In most cases this device is not installed and therefore not an issue

Notes or Warnings: None