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Mini Manual for PCI-ALTERA-PA3 created: 11/19/10

This mini-manual is for the HW differences between a standard PCI-Altera-LVDS and the PCI-Altera-PA3.

The PCI-Altera-LVDS is tested as an LVDS card and then modified by removing the last four LVDS transceivers [IO36-39] and replacing those with 4 discrete '125 drivers [SNLVC1G125DCKR]. The 4 added signals are TTL outputs which have tri-state control. Unlike the other TTL IO there are no pull-ups on these signals.

The '125 has a control pin active low, and a data input pin. The output pin is tied to the + side of the corresponding differential pair. The input pin is tied to the data signal that would have been used by the LVDS transceiver. The Control pin is tied to the direction pin that would have been used for the LVDS transceiver.

To transmit the direction signals should be in the low state. It is suggested that the design implement inverters so the reset state [if register driven] is off and a '1' written to the register enables.

The data transmitted will correspond to the standard data for that channel.

Please note the termination switches should be disabled for these signals.

Rework implemented at each LVDS site converted:

'125 **pins**	U45,47,48,49 **pads**	Signal
5	8	Power
4	6	output on + side of differential
3	5	Gnd
2	1,4	input to gate from IO
1	2,3	Cntl to gate from Dir

Note: pins separated by "," are options – pick one to make rework easier