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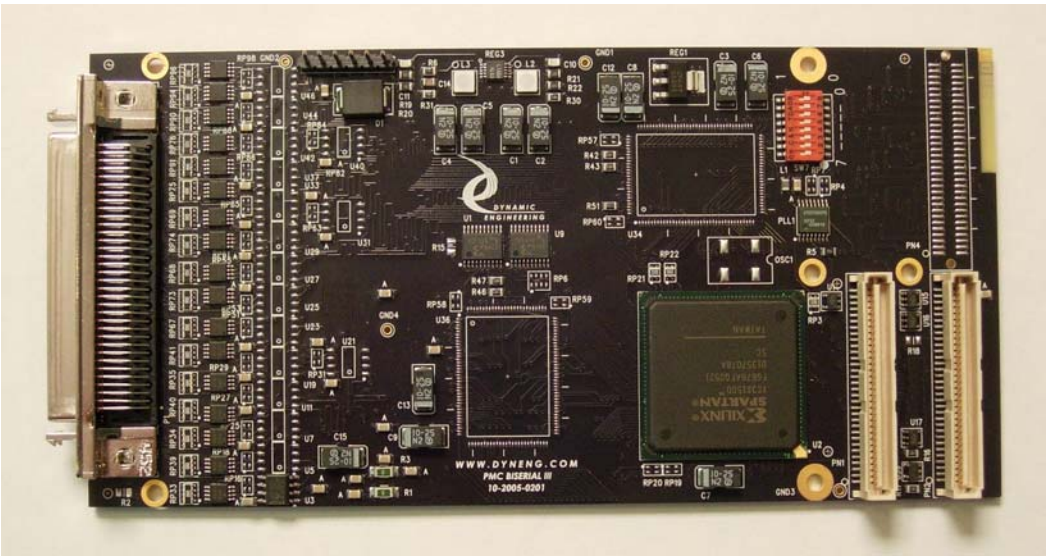
User Manual

PMC-BiSerial-III-OSEH

Bi-directional Serial Interface PMC Module



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PMC-BiSerial-III-OSEH
Bi-Directional Serial Data Interface
PMC Module

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Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

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Product Description

The PMC-BiSerial-III-OSEH is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-BiSerial-III is capable of providing multiple serial protocols. The OSEH protocol implemented provides a single transmit and receive channel each consisting of an RS-485 clock and data. The transmitter can use either an external clock reference, or an internal clock reference supplied by the on-board PLL.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a "standard" special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

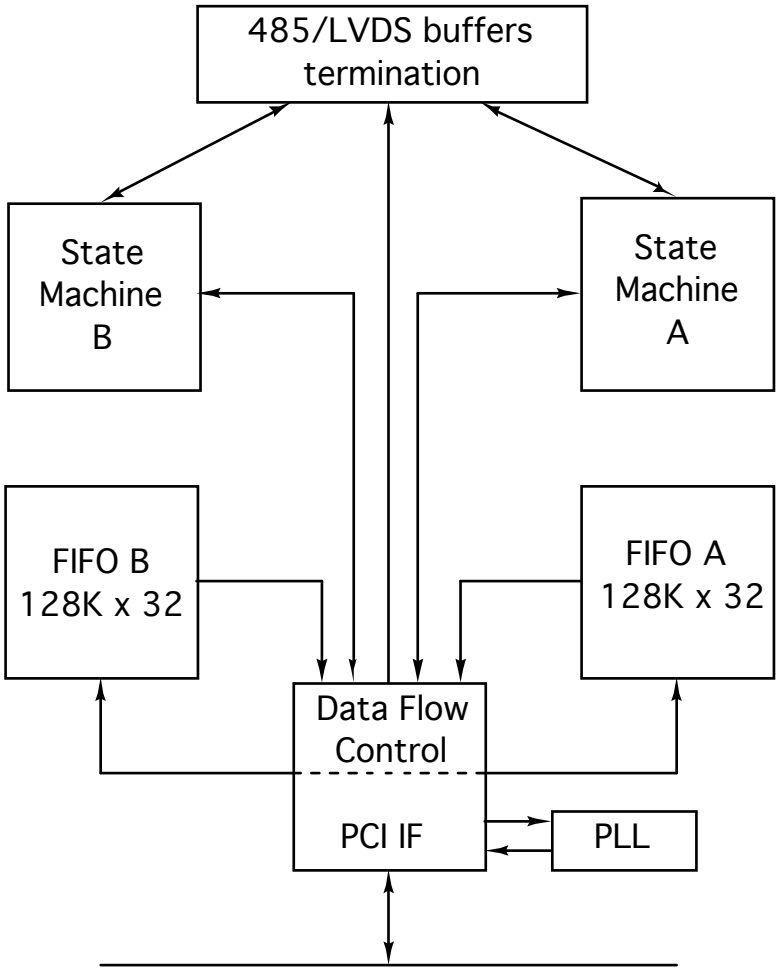


FIGURE 1 PMC-BISERIAL-III BLOCK DIAGRAM

The standard configuration shown in Figure 1 makes use of two external [to the Xilinx] FIFOs. The FIFOs can be as large as 128K deep x 32 bits wide. Most designs do not require so much memory, and are more efficiently implemented using FIFOs internal to the Xilinx FPGA.

The OSEH implementation has two 4K by 32-bit FIFOs using the Xilinx internal block RAM, one for the transmitter and one for the receiver. Data is transmitted LSB first in a continuous bit stream as long as the transmitter is enabled and data is present in the TX FIFO.

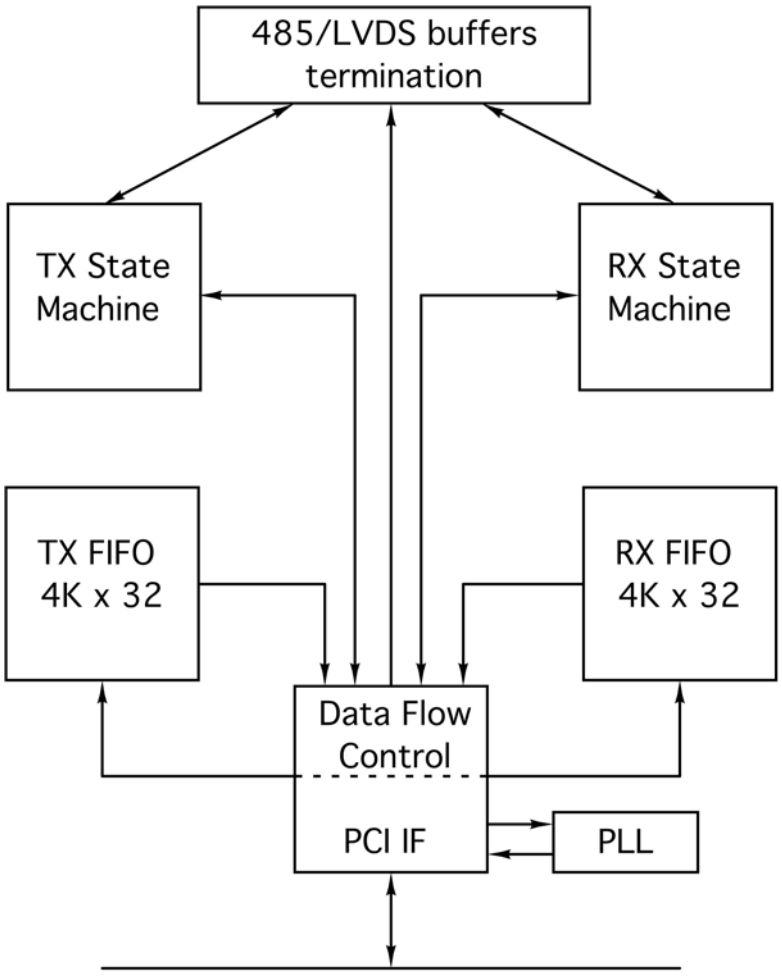


FIGURE 2 PMC-BISERIAL-III-OSEH BLOCK DIAGRAM

The data rate is derived from either an external clock reference or the on-board PLL A clock. The PLL is programmable and uses a 40 MHz reference oscillator to generate a wide range of frequencies. The target frequency for the design is a maximum frequency of 7 MHz, but should actually function at up to twice that rate.

Thirty-four differential I/O are provided at the front bezel for the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 100Ω. The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pullup/pulldown resistor packs can also be installed to provide a logic '1' on undriven lines.

This design uses only six of the I/O lines. The transmit section has an external clock reference input and a data and gated clock output. The receive section has a corresponding data and gated clock input as well as a clock reference output driven from the PLL B clock. The direction controls and the terminations for the input lines are fixed. The receiver section is present to test the transmit side, as this is the main focus for this design.

The PMC-BiSerial-III-OSEH conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The PMC-BiSerial-III-OSEH uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the PMC-BiSerial-III-OSEH, please let us know. We may be able to do a special build with a different height connector to compensate.

Various interrupts are supported by the PMC BiSerial-III-OSEH. An interrupt can be configured to occur at the end of a transmitted message. An interrupt can be set at the end of a received data-word. FIFO level interrupts and DMA complete interrupts are also supported. All interrupts are individually maskable, and a master interrupt enable is also provided to disable all interrupts simultaneously. The current status is available making it possible to operate in a polled mode when interrupts are disabled. All configuration registers support read and write

operations for maximum software convenience. All addresses are long word (32-bit) aligned.

Theory of Operation

The PMC-BiSerial-III-OSEH features a Xilinx FPGA. The FPGA contains all of the registers, FIFOs and protocol controlling elements of the PMC-BiSerial-III-OSEH design. Only the transceivers, switches and PLL circuit are external to the Xilinx device.

The PMC-BiSerial-III-OSEH is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. In standard configuration, the PMC-BiSerial-III-OSEH is a Type 1 mechanical with only low profile passive components on the back of the board, one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and basic logic design.

A logic block within the Xilinx controls the PCI interface to the host CPU. The PMC-BiSerial-III-OSEH design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decode before the "terminate with data" state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather DMA is provided for in this design. Once the physical address of the first chaining descriptor is written to the appropriate DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is set to one if the IO transfer is from the PMC-BiSerial-III-OSEH board to host memory, and zero if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

The PMC-BiSerial-III-OSEH sends data LSB first with no gaps between words. The clock is active only when valid data is being sent. The timing is shown in figure 2 below.

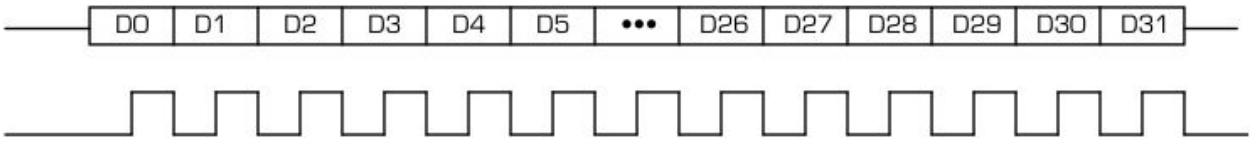


FIGURE 3 PMC BISERIAL-III-OSEH TIMING DIAGRAM

Either an internal or external clock reference is used to determine the TX data rate. The transmitter will continue to send data as long as it is enabled and there is data in the FIFO. When the FIFO becomes empty, a TX interrupt pulse is generated which will clear the TX enable bit unless this function is disabled.

The receiver clocks data into a 32-bit shift register using the gated clock input. When 32 bits have been received, the data word is written to the RX FIFO and the process continues. If the receive interrupt is enabled, an interrupt pulse will be generated for each word received.

TX FIFO almost empty and RX FIFO almost full interrupts can also be used. The levels at which these operate are programmable by writing values into the respective FIFO level registers. These values are also used to trigger DMA arbitration preemption when both input and output DMAs are simultaneously pending. This process helps to prevent RX FIFO overrun and TX FIFO underrun when data is being transferred in both directions at once.

Interrupts can also be triggered by the completion of a read or write DMA to facilitate data transfer efficiency.

Programming

Programming the PMC-BiSerial-III-OSEH requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial-III-OSEH "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to receive data the software is only required to enable the receiver. To transmit, the software will need to load the message into the TX FIFO, select the clock reference and enable the transmitter.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the FIFO level interrupts, the TX/RX interrupts, and/or the DMA completion interrupts. After an interrupt is received, new TX data can be written or RX data retrieved. An efficient loop can then be implemented to process the data. New messages can be sent or received even as the current one is in process.

If more than one interrupt is enabled, then the software needs to read the status to see which source caused the interrupt. The status bits are latched, and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

If DMA is to be used it will be necessary to acquire blocks of non-paged memory that is accessible from the PCI bus in which to store the chaining descriptor list entries.

Refer to the Theory of Operation section above and the register definition section below for more information regarding the exact sequencing and interrupt definitions.

Address Map

Register Name	Offset	Description
PB3_OSEH_BASE	0x0000	Base control register
PB3_OSEH_PLL_WRITE	0x0000	Base control - bits 16-19 used for pll control
PB3_OSEH_PLL_READ	0x0004	Switch port bit 19 used for pll_sdat input
PB3_OSEH_USER_SWITCH	0x0004	User switch read port
PB3_OSEH_TX_START_LAT	0x0008	TX start latch
PB3_OSEH_STATUS	0x000C	Status register
PB3_OSEH_STAT_CLEAR	0x000C	Status latch clear
PB3_OSEH_WR_DMA_PNTR	0x0010	Write DMA physical PCI dpr address
PB3_OSEH_RD_DMA_PNTR	0x0014	Read DMA physical PCI dpr address
PB3_OSEH_FIFO	0x0018	FIFO single word access
PB3_OSEH_TX_AMT_LVL	0x001C	TX almost empty level
PB3_OSEH_RX_AFL_LVL	0x0020	RX almost full level
PB3_OSEH_TX_FIFO_COUNT	0x0024	TX FIFO count
PB3_OSEH_RX_FIFO_COUNT	0x0028	RX FIFO count

FIGURE 4 PMC-BISERIAL-III-OSEH XILINX ADDRESS MAP

The VendorId = 0x10EE. The CardId = 0x0029.

Register Definitions

PB3_OSEH_BASE

[0x0000] Base Control Register (read/write)

Base Control Register

Data Bit	Description
31-20	Spare
19	PLL Sdata Output
18	PLL S2 Output
17	PLL Sclk Output
16	PLL Enable
15-14	Spare
13	FIFO Bypass Enable
12	FIFO Reset
11	External Clock Select
10	RX FIFO Almost Full Interrupt Enable
9	RX Interrupt Enable
8	RX Enable
7	TX Enable Clear Disable
6	TX FIFO Almost Empty Interrupt Enable
5	TX Interrupt Enable
4	TX Enable (read only)
3	Read DMA Interrupt Enable
2	Write DMA Interrupt Enable
1	Force Interrupt
0	Master Interrupt Enable

FIGURE 5 PMC-BISERIAL-III-OSEH BASE CONTROL REGISTER

All bits are active high and are reset on power-up or reset command, except PLL enable, which defaults to enabled (high) on power-up or reset.

Master Interrupt Enable: When this bit is set to a one all enabled interrupts (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one a system interrupt will occur provided the master interrupt enable is set. This is useful for interrupt testing.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA writes and reads respectively. The DMA interrupts are not affected by the Master Interrupt Enable.

TX Enable: This is a read only bit that reflects the state of the TX Start Latch.

TX Interrupt Enable: When this bit is set to a one, the transmit interrupt is enabled. A transmit interrupt will be asserted when the transmit FIFO becomes empty during a transmission by setting this bit, provided the master interrupt enable is asserted. When this bit is zero, the transmit interrupt is disabled.

TX FIFO Almost Empty Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level transitions from not almost empty to almost empty as specified by the level in the PB3_OSEH_TX_AMT_LVL register, provided the master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the status register.

TX Enable Clear Disable: When this bit is zero, the TX start latch will be automatically cleared by the TX interrupt pulse that occurs when the transmitter runs out of data. When this bit is one, the start latch will not be automatically cleared.

RX Enable: When this bit is set to a one the receive state-machine is enabled and will start to look for received serial data. When this bit is zero, the receive state-machine is disabled.

RX Interrupt Enable: When this bit is set to a one, the receive interrupt is enabled. A receive interrupt will be asserted, provided the master interrupt is enabled when at least one 32-bit word is received. When this bit is zero, the receive interrupt is disabled.

RX FIFO Almost Full Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level becomes equal or greater to the value specified in the PB3_OSEH_RX_AFL_LVL register, provided the master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the status register.

External Clock Select: When this bit is set to a one, the TX state machine will use the external clock reference for the transmit clock. When this bit is zero the

internal clock reference will be used. The internal clock comes from PLL clock A.
FIFO Reset: When this bit is set to a one, the transmit and receive FIFOs will be reset. When this bit is zero, normal FIFO operation is enabled.

FIFO Bypass Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without using the IO. When this bit is zero, normal operation is enabled.

PLL Enable: When this bit is set to a one, the signals used to program and read the PLL are enabled.

PLL Sclk/Sdata Output: These signals are used to program the PLL over the I2C serial interface. Sclk is always an output whereas Sdata is bi-directional. This is where the output value is specified. When Sdata is an input it is read from the User Switch Port.

PLL S2 Output: This is an additional control line to the PLL that can be used to select additional pre-programmed frequencies.

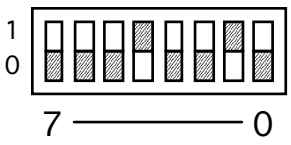
PB3_OSEH_USER_SWITCH

[0x0004] User Switch Port (read only)

Dip-Switch Port	
Data Bit	**Description**
31-20	Spare
19	PLL Sdata Input
18-16	Spare
15-8	Xilinx Design Revision Number
7-0	Switch Setting

FIGURE 6 PMC-BISERIAL-III-OSEH USER SWITCH PORT

Switch Setting: The user switch is read through this port. The bits are read as the lowest byte. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Xilinx Design Revision Number: The value of the second byte of this port is the rev. number of the Xilinx design (currently 0x02 - rev. B).

PLL Sdata Input: The PLL_sdata bi-directional line is read using this bit. This line is used to read the register contents of the PLL.

PB3_OSEH_TX_START_LAT

[0x0008] Control Latch (write only)

TX Start Latch	
Data Bit	**Description**
31-5	Spare
4	TX Enable (write only)
3-0	Spare

FIGURE 7 PMC-BISERIAL-III-OSEH TX START LATCH

TX Enable: When this bit is set to a one the transmit state-machine is enabled and will start to send serial data as soon as data is available in the TX FIFO. When this bit is zero, the transmit state-machine is disabled. This latch will be automatically cleared when the TX FIFO runs out of data unless the TX Enable Clear Disable bit in the Base Control register is set.

PB3_OSEH_STATUS

[0x000C] Status Read / Latch Clear Write Port

Status Register

Data Bit	Description
31	Local Interrupt Active
30-18	Spare
17	RX FIFO Almost Full Occurred
16	TX FIFO Almost Empty Occurred
15	Read DMA Interrupt Occurred
14	Write DMA Interrupt Occurred
13	Read DMA Error Occurred
12	Write DMA Error Occurred
11	Local Interrupt Condition Occurred
10	RX FIFO Overflow Occurred
9	RX Interrupt Occurred
8	TX Interrupt Occurred
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Spare
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 8 PMC-BISERIAL-III-OSEH STATUS PORT

Transmit FIFO Empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data words in the transmit data FIFO is less than or equal to the value written to the PB3_OSEH_TX_AMT_LVL register; when a zero is read, the level is more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive FIFO Empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data words in the receive data FIFO is greater or equal to the value written to the PB3_OSEH_RX_AFL_LVL register; when a zero is read, the level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO is empty, because as soon as the first four words are written into the FIFO, they are read out to be ready for a PCI read DMA or single word access. When this bit is a zero, it indicates that there is no valid receive data.

TX Interrupt Occurred: When a one is read, it indicates that the transmit state-machine sent some amount of data and then the TX FIFO became empty. A zero indicates that this condition has not occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

RX Interrupt Occurred: When a one is read, it indicates that the receive state-machine has received at least one 32-bit data-word. This bit will only be asserted if the RX Interrupt Enable is set in the Base Control register. A zero indicates that this condition has not occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

RX FIFO Overflow Occurred: When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. A zero indicates that no overflow condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Local Interrupt Condition Occurred: When a one is read, it indicates that an enabled local interrupt condition has occurred. These conditions include the TX and RX interrupts as well as the TX Almost Empty and RX Almost Full interrupts. Also the Force Interrupt bit will cause this bit to be asserted. A system interrupt will occur if the Master Interrupt Enable is set. A zero indicates that no enabled local interrupt condition is active.

Write DMA Error Occurred: When a one is read, a write DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is a one. A zero indicates that no write DMA error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Read DMA Error Occurred: When a one is read, a read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is a zero. A zero indicates that no read DMA error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Write DMA Interrupt Occurred: When a one is read, a write DMA interrupt is latched. This indicates that the scatter-gather list for the current write DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no write DMA interrupt is pending.

Read DMA Interrupt Occurred: When a one is read, it indicates that a read DMA interrupt is latched. This indicates that the scatter-gather list for the current read DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no read DMA interrupt is pending.

TX FIFO Almost Empty Occurred: When a one is read, it indicates that the transmit FIFO has become almost empty. A zero indicates that no TX FIFO almost empty has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

RX FIFO Almost Full Occurred: When a one is read, it indicates that the receive FIFO has become almost full. A zero indicates that no RX FIFO almost full has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Local Interrupt Active: When a one is read, it indicates that a system interrupt is asserted caused by an enabled local interrupt condition. A zero indicates that no system interrupt is pending from an enabled local interrupt condition

PB3_OSEH_WR_DMA_PNTR

[0x0010] Write DMA Pointer (write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 9 PMC-BISERIAL-III-OSEH WRITE DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather write DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer containing the data to write to the device, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

PB3_OSEH_RD_DMA_PNTR

[0x0014] Read DMA Pointer (write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 10 PMC-BISERIAL-III-OSEH READ DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather read DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer where the data from the device will be stored, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

PB3_OSEH_FIFO

[0x0018,] Write TX/Read RX FIFO Port

RX and TX FIFO Port	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 11 PMC-BISERIAL-III-OSEH RX/TX FIFO PORT

This port is used to make single-word accesses to the TX and RX FIFOs.

PB3_OSEH_TX_AMT_LVL

[0x001C] TX almost-empty level (read/write)

TX Almost-Empty Level Register	
Data Bit	**Description**
31-16	Spare
15-0	TX FIFO almost-empty level

FIGURE 12 PMC-BISERIAL-III-OSEH TX ALMOST EMPTY LEVEL REGISTER

This read/write port accesses the transmitter almost-empty level register. When the number of data words in the transmit data FIFO is equal or less than this value, the almost-empty status bit is set.

An interrupt may be generated if it is enabled when the FIFO level transitions from not almost-empty to almost-empty.

PB3_OSEH_RX_AFL_LVL

[0x0020] RX almost-full level (read/write)

RX Almost-Full Level Register	
Data Bit	**Description**
31-16	Spare
15-0	RX FIFO almost-full level

FIGURE 13 PMC-BISERIAL-III-OSEH RX ALMOST FULL LEVEL REGISTER

This read/write port accesses the receiver almost-full level register. When the number of data words in the receive data FIFO is equal or greater than this value, the almost-full status bit is set.

An interrupt may be generated if it is enabled when the FIFO level transitions from not almost-full to almost-full.

PB3_OSEH_TX_FIFO_COUNT

[0x0024] TX FIFO data count (read only)

TX FIFO Data Count Port	
Data Bit	**Description**
31-12	Spare
11-0	TX data words stored

FIGURE 14 PMC-BISERIAL-III-OSEH TX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the transmit FIFO (currently a maximum of 0xFFF).

PB3_OSEH_RX_FIFO_COUNT

[0x0028] RX FIFO data count (read only)

RX FIFO Data Count Port	
Data Bit	**Description**
31-12	Spare
11-0	RX data words stored

FIGURE 15 PMC-BISERIAL-III-OSEH RX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the receive FIFO (currently a maximum of 0xFFF).

Loop-back

The Engineering kit has reference software, which includes external loop-back tests. The PMC-BiSerial-III-OSEH has a 68 pin SCSI II front panel connector. The tests require an external cable with the following pins connected.

Signal	From	To	Signal
TX CLOCK+	pin 1	pin 17	RX CLOCK+
TX CLOCK+	pin 35	pin 51	RX CLOCK-
TX DATA+	pin 2	pin 18	RX DATA+
TX DATA-	pin 36	pin 52	RX DATA-
EXT CLOCK+	pin 3	pin 19	CLOCK REF+
EXT CLOCK-	pin 37	pin 53	CLOCK REF-

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BiSerial-III-OSEH. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 16 PMC-BISERIAL-III-OSEH PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BiSerial-III-OSEH. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 17 PMC-BISERIAL-III-OSEH PN2 INTERFACE

BiSerial III Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC BiSerial-III-OSEH. Also, see the User Manual for your carrier board for more information. For customized version, or other options, contact Dynamic Engineering.

IO_0p (TX CLOCK+)	IO_0m (TX CLOCK-)	1	35
IO_1p (TX DATA+)	IO_1m (TX DATA-)	2	36
IO_2p (EXT CLOCK+)	IO_2m (EXT CLOCK-)	3	37
IO_3p	IO_3m	4	38
IO_4p	IO_4m	5	39
IO_5p	IO_5m	6	40
IO_6p	IO_6m	7	41
IO_7p	IO_7m	8	42
IO_8p	IO_8m	9	43
IO_9p	IO_9m	10	44
IO_10p	IO_10m	11	45
IO_11p	IO_11m	12	46
IO_12p	IO_12m	13	47
IO_13p	IO_13m	14	48
IO_14p	IO_14m	15	49
IO_15p	IO_15m	16	50
IO_16p (RX CLOCK+)	IO_16m (RX CLOCK-)	17	51
IO_17p (RX DATA+)	IO_17m (RX DATA-)	18	52
IO_18p (CLOCK REF+)	IO_18m (CLOCK REF-)	19	53
IO_19p	IO_19m	20	54
IO_20p	IO_20m	21	55
IO_21p	IO_21m	22	56
IO_22p	IO_22m	23	57
IO_23p	IO_23m	24	58
IO_24p	IO_24m	25	59
IO_25p	IO_25m	26	60
IO_26p	IO_26m	27	61
IO_27p	IO_27m	28	62
IO_28p	IO_28m	29	63
IO_29p	IO_29m	30	64
IO_30p	IO_30m	31	65
IO_31p	IO_31m	32	66
IO_32p	IO_32m	33	67
IO_33p	IO_33m	34	68

FIGURE 18 PMC-BISERIAL-III-OSEH FRONT PANEL INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD

Proper ESD handling procedures must be followed when handling the PMC-BiSerial-III-OSEH. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up

Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds

All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BiSerial-III-OSEH is constructed out of 0.062-inch thick FR4 material.

Through-hole and surface-mount components are used. The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-BiSerial-III-OSEH design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
support@dyneng.com

Specifications

Host Interface:	[PMC] PCI Mezzanine Card – 32-bit, 33 MHz
Serial Interfaces:	Two serial interfaces (one in and one out). 32-bit word size, LSB first, multiple words, reference clock, data and gated clock
TX Bit-rates generated:	≤ 7 MHz for TX and RX serial channel, internal and external clock references for TX
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	TX FIFO almost empty, RX FIFO almost full, TX done, RX data received, read, and write DMA done
DMA:	Scatter/Gather DMA Support implemented
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Through-Hole and Surface-Mount Components
Temperature Coefficient:	2.17 W/ºC for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V
Temperature range	Standard (0 to +70) Extended Temperature available (-40 to +85)

Order Information

PMC-BiSerial-III-OSEH	PMC Module with 2 serial channels, RS-485 IO, 32-bit data interface
Eng Kit PMC-BiSerial-III-OSEH	HDEterm68 - 68 position screw terminal adapter http://www.dyneng.com/HDEterm68.html HDEcabl68 - 68 IO twisted pair cable http://www.dyneng.com/HDEcabl68.html Technical Documentation, 1. PMC-BiSerial-III Schematic 2. PMC-BiSerial-III-OSEH Driver software and user application. Data sheet reprints are available from the manufacturer's web site

***Note**: The Engineering Kit is strongly recommended for first time* PMC BiSerial-III *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.