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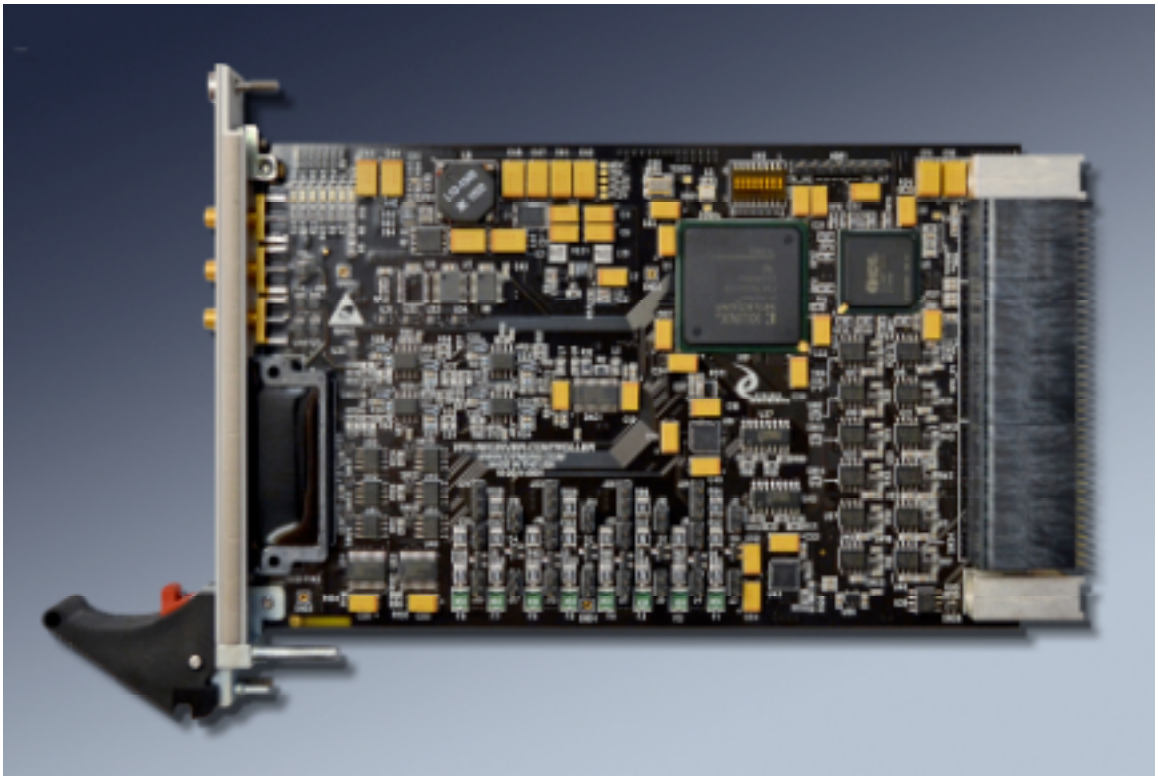
User Manual

VPX Receiver Controller Board

VPX 3U 4HP



Revision A1
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VPX Receiver Controller
3U 4HP

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Product Description

VPX Receiver Controller is part of the Dynamic Engineering VPX compatible family of modular I/O components.

The VPX Receiver Controller is a 3U 4HP design optimized for the control of a specific digital receiver. Multiple SPI buses, A/D, D/A, clock references and special purpose IO are provided to support the receiver.

The PCI interface is implemented within a Spartan 3 FPGA. The control logic for the receiver and related interface hardware is also done within the FPGA.

Special features:

- Universal VPX 3U 4HP
- SPI for Receiver “RS”
- SPI for Calibration Source “CS”
- SMB for Monitor function
- SPI for D/A – 8 channel D/A on board plus inverting buffers for attenuation control, 2 per RF/IF Module connector
- SPI for communication with CPU
- 5V power from VPX used to generate 1.2, 2.5, -5
- 10 MHz clock reference LVTTL SMA x3
- Misc Signal conversion to support CPU LVDS ⇔ RS485.
- DIP Switch for positive board identification
- Signal conditioning for high voltage inputs. Programmable resistor network plus comparators.
- Dual access registers for SPI and PCIe control as desired

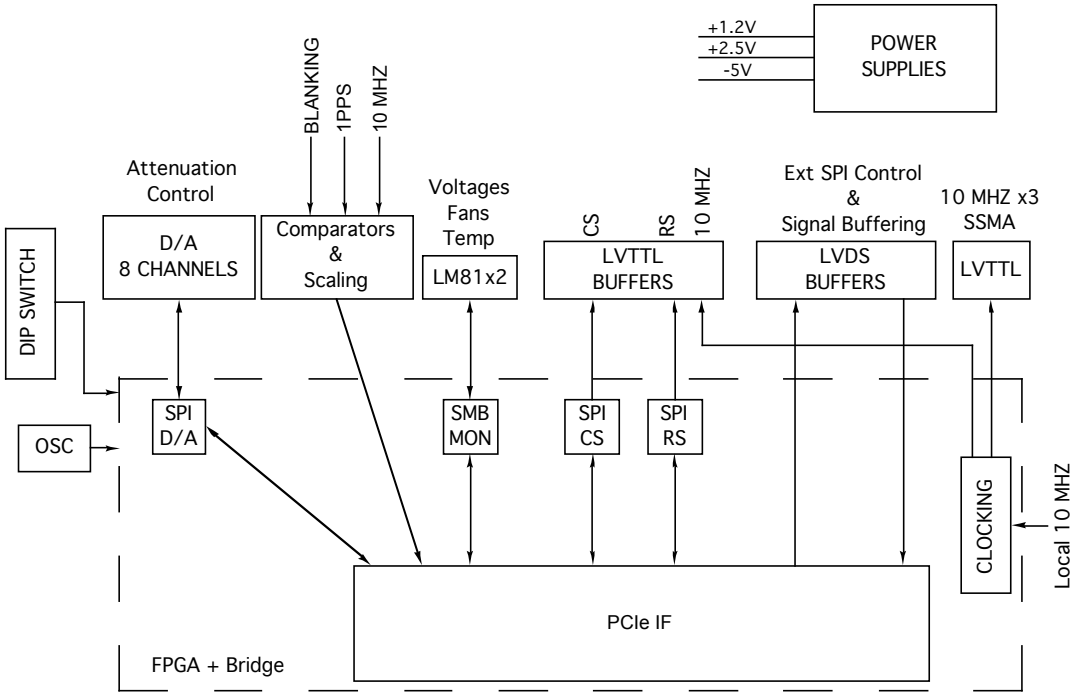


FIGURE 1 VPX RCB BLOCK DIAGRAM

The Receiver Controller has many features and many details to cover. An outline of the features and basic capabilities is provided in this section of the manual. The detailed programming and use information is in the next section.

The diagram is simplified. Most of the interfaces shown have control and data registers. The register map is direct.

VPX-RCB can be controlled via PCIe or SPI or both. The registers used by the SPI interface are also accessible from the PCIe port. The SPI interface with the CPU is received and decoded. SPI accesses to internal functions are re-routed to a second decoder which extracts data to be written or packages data to be read. The extracted data is stored into a local register and then parallel loaded to the target register. The size of the data is programmable within the VHDL. Messages of incorrect length are filtered – keeping the initial message and dumping the extra clocks. Each of the local registers has a separate data path [parallel] back to the encoder/decoder. The address received selects the mux output desired and the state-machine returns the requested data.

Functions that are external to the FPGA are routed there directly. The timing for those accesses are controlled by the CPU.

VPX-RCB has an 8 position DIP Switch installed. The DIP Switch is not used for any feature selection. The DIP Switch is available for software defined purposes. A suggested use is for differentiation of multiple Receiver Controller boards within the system.

The FPGA receives 50 MHz from the oscillator. The clock input is doubled to 100 MHz and used locally for decoding SPI signaling and operating miscellaneous state-machines. A TXCO oscillator at 10 MHz provides a local reference. The local reference is compared with the external clock reference received through the comparators. Software can select the internal or external reference to be driven to the three SSMA connectors at the bezel.

The internally generated 10 MHz is supplied to a counter in parallel with a second counter referenced to the external 10 MHz. The software can reset, start, and set the end count for the internally referenced counter. For example the software can set a count corresponding to 1 mS of time counting. In addition upper and lower limits can be programmed. At the end of the test the value counted is checked against the limits and status is generated. Passing status is between the limits. An interrupt can be generated to the CPU through the attention signal if the status changes. The test starts and runs automatically. The compared values and end counts are buffered and synchronized to allow changes to happen at any time. The values changes are implemented synchronicity as well. The new values will be applied at the next opportunity for a check etc.

The Maxim 5593 10 bit DAC is used for the 8 channels of D/A conversion. An SPI interface converts the data written to the control register to SPI format and sends it to the DAC. The DAC outputs a voltage corresponding to the programmed value. The system requires a voltage range of 0 to –3V. Inverting buffers are used to change the range of the signal. Each of the outputs is coupled through a 100Ω resistor. The 8 outputs are tied to the 69 pin high density connector.

In addition to the data bits there are 4 control bits to select the mode of the programming. Several features built into the 5593 are interesting. Output on one channel, output to multiple channels, etc.

LM81 is a monitor circuit controlled with the SMB bus. The FPGA converts the

SPI bus to SMB format. The LM81 is initialized for operation and then interrogated for Voltage levels, Fan speeds, and temperature. The device uses A/D's to load the conversion values into memory. The LM81 stops updating when a value is read. It takes the better part of a second to update again. It is best to do a burst read of any values you are interesting in and then wait for the system requirement before doing it again. The LM81's can be programmed with upper and lower limits for each of the measurements and alarms generated if the values are out of bounds.

The Calibration Source and Receiver have identical and separate SPI interfaces. The master SPI interface from the CPU is routed to the correct device based on the address bits presented in parallel with the clock and data lines of the SPI bus. The decoding also affects when to access the other functions of the card.

Address Map

Name	Offset	Function
VpxRcb_BASE_BASE	0x0000 // 0	VpxRcbBase Base control register
VpxRcb_BASE_USER_SWITCH	0x0004 // 1	VpxRcbBase User switch read port
VpxRcb_BASE_XILINX_REV	0x0004 // 1	VpxRcbBase Xilinx revision read port
VpxRcb_BASE_XILINX_DES	0x0004 // 1	VpxRcbBase Xilinx design read port
VpxRcb_BASE_PCI_REV	0x0004 // 1	VpxRcbBase PCI Core Revision
VpxRcb_BASE_SPI_0	0x0008 // 2	VpxRcbBase SPI Register offset 0 11 bits
VpxRcb_BASE_SPI_1	0x000C // 3	VpxRcbBase SPI Register offset 1 11 bits
VpxRcb_BASE_SPI_2	0x0010 // 4	VpxRcbBase SPI Register offset 2 24 bits check count lower
VpxRcb_BASE_SPI_3	0x0014 // 5	VpxRcbBase SPI Register offset 3 24 bits check count upper
VpxRcb_BASE_SPI_4	0x0018 // 6	VpxRcbBase SPI Register offset 4 24 bits clock check count
VpxRcb_BASE_COUNT_E	0x001C // 7	VpxRcbBase Read Actual count from external 10 mhz
VpxRcb_BASE_COUNT_T	0x0020 // 8	VpxRcbBase Read Actual count from TCXO (internal) 10 mhz
VpxRcb_BASE_SPI_5	0x0024 // 9	VpxRcbBase SPI Register offset 5 12 bits Antenna control
VpxRcb_BASE_SPI_6	0x0028 // 10	VpxRcbBase SPI Register offset 6 12 bits SMB data in
VpxRcb_BASE_SPI_7	0x002C // 11	VpxRcbBase SPI Register offset 7 8 bits POT programming
VpxRcb_BASE_SPI_TEST	0x0030 // 12	VpxRcbBase SPI TEST Register offset mimic SPI commands using PCIe bus based commands

VendorID = xDCBA
CardID = x0047

The Vendor and Card ID's can be used to determine the correct handle with your driver when using the PCIe based control path. The SPI control path is hardwired and local addresses used to select the device and functions within the device. Please see the VpxRcb_BASE_SPI_TEST description for more information.

Bit Maps

VpxRcb_BASE_BASE

0x0000 // 0 base control register offset

Bits	Function
15–6	unused
5	F_INT
4	M_INT_EN
3-0	unused

M_INT_EN is the board level Master Interrupt Enable. When ‘1’ interrupts can be generated by the board. When ‘0’ interrupts are masked off.

F_INT is the Force Interrupt bit. When set and the master is enabled the design will cause an interrupt request to the system. Clear by setting to ‘0’. Default is ‘0’. Main purpose is to allow software programmed interrupts for testing purposes.

VPX_rcvrcntl_ID

0x0004 // 1 ID Register offset

Bits	Function
31-24	Design Revision
23-16	Design ID
15-8	Xilinx Revision
7-0	DIP Switch

The Xilinx Revision is currently set to 0x01. The revision will be updated as new features are added to allow software differentiation. The Xilinx revision is also visible from the configuration space within the PCI status.

The design ID is also set to 0x01 for this initial version of the RCB. If new incompatible design changes are made the design ID will be changed and the CardID will also be changed.

The DIP Switch is read directly from this port. The value read matches the settings on the switch. The Switch is defined on the silkscreen for bit and 1,0.

VpxRcb_BASE_SPI_0 Write

0x0008 // 2 Register offset

Bits	Function
31	Interrupt – read only
30-11	undefined
10	ClockSelect
9-8	spare
7	Clear Attention Lock Rx Lo
6	Clear Attention Cal Src Lo
5	Clear Attention Ext 10 MHz Status
4	Clear Attention TCXO status
3	Enable COS Lock Rx Lo
2	Enable COS Cal Src Lo
1	Enable COS Ext 10 MHz Status
0	Enable COS TCXO status

Read-back from the PCIe interface is the same as writing from the PCIe or SPI interface. The SPI port has an alternate read-back definition. The size of the SPI port for read and write is “B”. The SPI address is Internal 0.

When set the Enable COS bits capture changes in status to create an attention signal to the host CPU. The clear bits when set clear the captured status. The clear bits are captured by the register, but only used during the register write and are momentary as a result. If the Enable is left “enabled” the clear will remove the cause of the attention signal and return to scanning for more changes. If the signal is not wanted for COS attention operation it must be disabled.

The Clock Select bit is used to select the internal TCXO source ‘0’ or the external received clock ‘1’. The clock selected is used to drive the three coax signals via bezel connectors.

Interrupt is the combination of potential masked interrupt requests. When set an interrupt request is pending from the card. When ‘0’ no interrupt is pending. Interrupt is used for determining the source of a request in a shared interrupt environment.

VpxRcb_BASE_SPI_0 Read

0x0008 // 2 Register offset

Bits	Function
23-11	undefined
10	ClockSelect
9-8	spare
7	Receiver 1st Lo Lock N
6	Cal SRC 1st Lo Lock N
5	External Clock Count Valid
4	TCXO Clock Count Valid
3	Enable COS Lock Rx Lo
2	Enable COS Cal Src Lo
1	Enable COS Ext 10 MHz Status
0	Enable COS TCXO status

Clock Select is the read-back of the clock select bit defined in the Write section.

Receiver 1st Lo Lock N and Cal SRC 1st Lo Lock N are the raw status used for the COS inputs.

The Count Valid status bits are the “real time” status for the clocks based on the programmed limits. If the count is within the range set, the status will be valid. Status is based on counting for the programmed length of time [number of counts]. The count status is updated based on the programmed length. The

current count status is displayed until the next measurement is completed. The measurements are continuous.

The enable COS bits allow read-back of the current state of the control bits.

VpxRcb_BASE_SPI_1

0x000C // 3 RS485 Control Register offset

Bits	Function
31-11	undefined
10	Force Attn
9	Sel FP
8	SelTxRx
7	DirRs485Rx
6	DirRs485Tx
5	DirRs485RxFp
4	DirRs485TxFp
3	TermRs485Rx
2	TermRs485Tx
1	TermRs485RxFp
0	TermRs485TxFp

Read-back from the PCIe interface is the same as writing from the PCIe or SPI interface. The SPI port for this register matches the write port. The size of the SPI port for read and write is “B”. The SPI address is Internal 1.

TermRs485TxFp when set ‘1’ asserts termination on the Rs485 buffer normally used for Transmit at the Front panel. [J1-12, 9]

DirRs485TxFp when set ‘1’ sets the direction to transmit on the Rs485 buffer normally used for Transmit at the Front panel. [J1-12, 9]

TermRs485RxFp when set ‘1’ asserts termination on the Rs485 buffer normally used for Receive at the Front panel. [J1-10, 7]

DirRs485RxFp when set ‘1’ sets the direction to transmit on the Rs485 buffer normally used for Receive at the Front panel. [J1-10, 7]

TermRs485Tx when set ‘1’ asserts termination on the Rs485 buffer normally used for Transmit at the rear IO connector. [P2-B16, C16]

DirRs485Tx when set ‘1’ sets the direction to transmit on the Rs485 buffer normally used for Transmit at the rear IO connector. [P2-B16, C16]

TermRs485Rx when set ‘1’ asserts termination on the Rs485 buffer normally used for Receive at the rear IO connector. [P2-E16, F16]

DirRs485Rx when set ‘1’ sets the direction to transmit on the Rs485 buffer normally used for Receive at the rear IO connector. [P2-E16, F16]

SelTxRx: When ‘0’ use the Rx port to receive. When ‘1’ use the Tx port to receive.

Sel FP: When ‘0’ select the Rear [P2] IO and when ‘1’ select the FP [J1] IO.

The RS485 IO as defined will be used to buffer the LVDS IO to/from the host CPU on DP 7 and 8 of P2.

Force Attn. When set ‘1’ causes the Attention bit to be set. Useful for self test purposes and software development

VpxRcb_BASE_SPI_2

0x0010 // 4 Register offset

Bits	Function
31-24	undefined
23-0	Clock Check Lower

VpxRcb_BASE_SPI_3

0x0014 // 5 Register offset

Bits	Function
31-24	undefined
23-0	Clock Check Upper

VpxRcb_BASE_SPI_4

0x0018 // 6 Register offset

Bits	Function
31-24	undefined
23-0	Clock Check Count

Read-back from the PCIe interface is the same as writing from the PCIe or SPI interface. The SPI ports for these registers matche the respective write ports. The size of the SPI ports for read and write is “18”. The SPI addresses are Internal 2-4.

Count Check Lower is used to determine if the accumulated count is too low. Count Check Upper is used to determine if the accumulated count is too high. Clock Check Count is used to define the measurement period.

The 100 MHz. internal reference is used to count up to the programmed Clock Check Count. When the terminal count is reached the accumulated counts on the TCXO and External clock references are checked against the limits. If within the limits the status is set ‘1’. If not the status is cleared ‘0’. The Status remains in the determined state until the next measurement is completed. The status is meaningless until the limits and count period are established. The COS bits should not be enabled until the limits and period are programmed and the hardware has a chance to do at least 1 period as programmed.

The limits are not included in the range [GT lower limit and LT upper limit is definition of “good” status].

Since the 100 MHz reference is faster than the 10 MHz expected rate be sure to use a large enough count to capture several counts on the 10 MHz.

The userap supplied with the driver has example code for programming these registers and checking the status,

VpxRcb_BASE_COUNT_E

0x001C // 7 Register offset Read Only

Bits	Function
31-25	undefined
24	External Status
23-0	External Count

VpxRcb_BASE_COUNT_T

0x0020 // 8 Register offset Read Only

Bits	Function
31-25	undefined
24	TCXO Status
23-0	TCXO Count

The PCIe interface supports the read-back of the actual counts captured for the clcok check test. The counts are updated once per period. The counts are stable as they are double buffered. The counts may be read at any time and the last completed count retrieved. If the read rate is faster than the programmed period for the test the same data will be returned multiple times before being updated.

Bit 24 is the status as determined by the counting system. A '1' means the count is within the bounds set with the lower and upper limit registers when the total count was achieved by the 100 MHz. counter.

VpxRcb_BASE_SPI_5

0x0024 // 9 Register offset

Bits	Function
31-12	undefined
11	Ant Array Data
10	Ant Sel0 Data
9	Ant Sel1 Data
8	Ant Sel2 Data
7	Ant Array Dir
6	Ant Sel0 Dir
5	Ant Sel1 Dir
4	Ant Sel2 Dir
3	spare
2	spare
1	spare
0	Cal Switch

Read-back from the PCIe interface is the same as writing from the PCIe or SPI interface. The SPI port for this register matches the write port. The size of the SPI port for read and write is "C". The SPI address is Internal 5.

Cal Switch is re-driven to the bezel connector.

Ant xxx Dir when set = transmit, when cleared = receive. It is expected the direction is transmit, terminations are set to off. The terminations can be made to be programmable if this changes.

Ant xxx Data are tied to the corresponding front panel ANT SEL lines via RS485 buffers. Software timing on this interface. Due to the intermediate parallel load of the registers the outputs will be synchronous with each other.

VpxRcb_BASE_SPI_6

0x0028 // 10 Register offset Read / Write

Bits	Function
31-12	undefined
11	SMB TCRIT1N/Clear SMB TCRIT1N
10	SMB TCRIT0N/Clear SMB TCRIT0N
9	SMB INT1N/Clear SMB INT1N
8	SMB INT0N/Clear SMB INT0N
7	'0'/spare
6	SMB Reset
5	spare
4	spare
3	Attn En SMB TCRIT1N
2	Attn En SMB TCRIT0N
1	Attn En SMB INT1N
0	Attn En SMB INT0N

Read-back from the PCIe interface is the same as writing from the PCIe or SPI interface. The SPI read port for this register is different than the write port. The size of the SPI port for read and write is "C". The SPI address is Internal 6.

Items without the "/" are the same definition for read and write. Items with the "/" are different with the read / write definitions shown.

SMB Reset is driven low with SMB Reset is '1' otherwise tristated to allow the external pull-up to take out of reset. Reset can be used to return the LM81's to a known state if your software has shutdown in the middle of an operation etc.

The Attn En bits are set '1' to enable the corresponding signals to cause the Attention bit to the host CPU to be set.

The Clear bits are used to clear the held status captured with the COS logic.

The SMB signals are the status bits from the LM81's for interrupt and temperature critical. The interrupt and temperature behavior is programmable within the LM81's. Please refer to the LM81 data sheet for those details.

Examples of interacting with the LM81 are contained in the UserAp software. The LM81 has many registers. The .H file may save some typing time as many of the registers are defined in the Ddxxx.H file.

VpxRcb_BASE_SPI_7

0x002C // 11 Register offset Read / Write

Bits	Function
31-8	undefined
7-0	POT Data

Read-back from the PCIe interface is the same as writing from the PCIe or SPI interface. The SPI read port for this register is the same as the write port. The size of the SPI port for read and write is "8". The SPI address is Internal 7.

Writing from the SPI or PCIe interface with store the byte of data to program into the Digital Potentiometer and start the transmit state machine. The POT is programmed with 0-FF corresponding to a range of –5V ⇔ +5V for the revision 2 board. For revision 1 the range is 0V-5V. Bit 7 serves as a sign bit.

The output from the Digital POT is used as a programming option for the Blanking comparators. When a differential input is available make that selection with J21-24 [1-2] [BLANK0-3]. When a non differential input is available select 2-3 on the header and program the reference level as appropriate. Please see the headers and shunts section for the rest of the Blanking input shunt programming options.

VpxRcb_BASE_SPI_TEST

0x0030 // 12 Register offset

Bits	Function
31-9	undefined
8	TMiso (read only)
7	TSel
6	TDevSel2
5	TDevSel1
4	TDevSel0
3	TEn
2	unused
1	TMosi
0	TClk

This is a PCIe only register. Access is used to control the Spare LVDS IO. In our test set-up we use the Spare LVDS IO to generate an SPI interface which we loop-back to the SPI port on P2. To facilitate the loop-back and PCIe access the PCIe2VPX3UX4 was used along with an HDEterm68. Both of these cards are available from Dynamic Engineering. Please see our website for card descriptions.

The register is used for “bit banging” to generate the SPI interface for test purposes.

Tsel is unused for the external loop-back part implementation. An internal loop-test was used initially and this bit was used to select the external SPI or the internal SPI. The current design is hardwired to use the external SPI interface.

TMosi is tied to the MOSI [master out slave in] signal to write data to VPX-RCB.

TMiso is the return data path from VPX-RCB and is tied to MISO through the loop-back described above and documented in the loop-back section.

TEn when set enables the Stearing logic to use the encoded address to drive a particular bus.

TDevSelx are used to set the 1st level address for the SPI bus. The first level is used by VPX-RCB to interconnect the SPI bus with the correct hardware. Within the SPI message can be further address and data information to be decoded by the target device.

Address	Destination
0	Local
1	Local
2	SMB
3	D/A
4	Cal Src 0
5	Cal Src 1
6	Rcvr Lo 0
7	Rcvr Lo 1

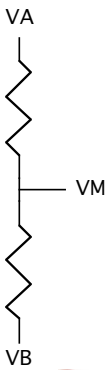
The local addresses within the VPX-RCB are decoded from the DevSel 0 or 1. The upper address range is not used at the moment. The first 8 registers are used from the lower range (0).

The local SPI interface protocol is based on an initial byte of local address followed by the data to write or the data read back. There is a 1 clock delay for the read data. The lengths for each of the registers are shown in the various bit map descriptions. The hardware is set-up to allow quick changes for register lengths.

The SMB bus is half duplex while the SPI is full duplex. VPX-RCB takes care of the expansion / multiplexing automatically. Remember to keep MOSI high when not transmitting and selecting the SMB bus.

The LM81's are on the SMB bus. The addresses are 0 and 1. The device at address 0 has the internal voltages plus connections for FAN0 and FAN1. 12, 5, 3.3, 2.5V are measured on the standard pins. Vccp1 is used to measure –5V.

The range of the VCCp input is not sufficient to measure –5V directly.



3.3V (VA) is tied through a 30.1K resistor (R1) to 90.90K (R2) to –5V (VB) with the node between (VM) the resistors going to the VCCp1 input.

It is suggested that the 3.3V measurement be taken first and then used when calculating the –5V value. The math is in the LM81 data sheet and a reference for programming in the userap software.

The LSB size is different for the different inputs for the LM81 based on the scaling in place within the device. 13mV for 2.5, 17.2mV for 3.3V, 26 mV for 5V, 62.5mV for 12V, and 14.1mV for the VCCp inputs.

The second device is on address 1. FAN2 and FAN3 are tied to the tach inputs. The following voltages are measured:
External 12 and 5 are measured on the 12 and 5V inputs directly.
+16 is measured on the 3.3V input: VA = 16, VB = GND, R1 = 53.6K, R2 = 14K.
+15 is measured on the 2.5V input: VA = 15, VB = GND, R1 = 49.9K, R2 = 10K.
-15 is measured on the VCCp1 input: VA = 3.3, VB = -15, R1 = 30.1K, R2 = 249K.
+7 is measured on the VCCp2 input: VA = 7, VB = GND, R1 = 17.4K, R2 = 6.04K.

All resistors are 1%. Some are combinations where the parallel / series value is shown.

VPX_rcvrcntl_DAC

Bits	Function
15-0	DAC Data

The Maxim 5593 8 channel DAC is used to set a reference voltage for the Attenuators. The value programmed onto the DAC outputs is inverted with an opamp. The DAC channels 7-0 correspond to the Attenuators 0-7.

The DAC is programmed as an external device in this design. The DAC is physically on the VPX-RCB but located outside of the FPGA. The SPI bus is used to program the device by selecting the external address and providing the "bit banged" data stream to the DAC channels.

The DAC used is available as a 12 or 10 bit device. The command structure is designed to work with several models including a 12 bit version. The upper 4 bits are control and the lower 12 are data. Data is MSB aligned and zero's are added to the LSB side where shorter control words are used.

Bit 15-12 = Control C3-C0
Bit 11-0 = Data, in the 10 Bit case D11-D2 are valid and D1,D0 are set to 0.

C3-C0
0000 outputs unchanged, load register A
0001 outputs unchanged, load register B
0010 outputs unchanged, load register C
0011 outputs unchanged, load register D
0100 outputs unchanged, load register E
0101 outputs unchanged, load register F
0110 outputs unchanged, load register G
0111 outputs unchanged, load register H

1000 plus DATA select output register(s) to update from stored shift register data
1001 load all input registers from shift register output unchanged - parallel value load
1010 load all input and output registers from common input.

Other control options exist to program slew rates and so forth. Please refer to the Maxim 5590-5595 data sheet for more information.

Headers and Shunts

VPX-RCB has a number of options. Many of the options are software selectable and some require shunts used with headers.

The Blanking inputs can be high or low voltage, single ended or differential. As a result a comparator with several scaling resistor options and offset voltages are provided.

Page 5 of the schematic has the circuit.

Signal+ FUSE 4.7K 1K comparator + input
Signal- FUSE 4.7K 1K comparator - input
The resistors are 1/2 W
The fuse is 140 mA rated
Each of the resistors is shuntable to take it out of the circuit.
Each of the signals is Diode coupled to +5 and –5 to keep it within range of the comparitor.

BLANK0 uses J2 and J4 for the 4.7K resistor – shunt to remove the resistor open to use the resistor.
BLANK0 uses J3 and J8 for the 1K resistor – shunt to remove the resistor open to use the resistor.
BLANK0 uses J21 to select a 100Ω parallel termination or the Digital Pot programmed reference voltage. 1-2 selects parallel, 2-3 selects the Pot.

BLANK1 uses J9 and J11 for the 4.7K resistor – shunt to remove the resistor open to use the resistor.
BLANK1 uses J10 and J12 for the 1K resistor – shunt to remove the resistor open to use the resistor.
BLANK1 uses J22 to select a 100Ω parallel termination or the Digital Pot programmed reference voltage. 1-2 selects parallel, 2-3 selects the Pot.

BLANK2 uses J13 and J15 for the 4.7K resistor – shunt to remove the resistor open to use the resistor.
BLANK2 uses J14 and J16 for the 1K resistor – shunt to remove the resistor open to use the resistor.
BLANK2 uses J23 to select a 100Ω parallel termination or the Digital Pot programmed reference voltage. 1-2 selects parallel, 2-3 selects the Pot.

BLANK3 uses J17 and J19 for the 4.7K resistor – shunt to remove the resistor

open to use the resistor.
BLANK3 uses J18 and J20 for the 1K resistor – shunt to remove the resistor open to use the resistor.
BLANK3 uses J24 to select a 100Ω parallel termination or the Digital Pot programmed reference voltage. 1-2 selects parallel, 2-3 selects the Pot.

The signals are converted to LVTTL with a combination of the comparator [LMH7324] and LVDS to LVTTL translator. The single ended signals are routed to the FPGA. For the moment the signals are re-routed to LVTTL to LVDS translators and driven to the host CPU.

The fan 12V is supplied for the LM81 [address 1] to measure. In addition a reference ground is supplied. R142 is used to tie the external 12V ground to the local ground. If AC coupling is desired this device can be switched out for a .1uF or similar 0603 capacitor or left open.

Loop-back

VPX-RCB uses a high density front panel connector, the rear IO J2 connector, and 3 coax connectors for the IO. With the PCIe2VPX3UX4 support board J2 IO is accessible for loop-back.

Initial testing was accomplished using local loop-back – local to the VPX. A PMC BiSerial III is used currently for loop-back tests and a more complete solution.

J2 has a spare 7 bit port which is looped-back to the SPI port to allow simulated control.

HDEterm68 plus a SCSI cable were used to create the loop-back "cable". HDEterm68 incorporates the same numbering as the PCIe2VPX3U64 on the wire-wrap headers allowing for easy to incorporate connections.

The mapping is as follows: [Standard pins looped to Spares of same name]

RCB	PCIe2VPX3UX4	Signal Name
A1	32	SPI CLK P
B1	66	SPI CLK N
D1	31	MOSI P
E1	65	MOSI N
B2	30	MISO P
C2	64	MISO N
E2	29	SPI DEV SEL 0 P
F2	63	SPI DEV SEL 1 N
A3	28	SPI DEV SEL 1 P
B3	62	SPI DEV SEL 1 N
D3	27	SPI DEV SEL 2 P
E3	61	SPI DEV SEL 2 N
B4	26	SPI DEV ENA P
C4	60	SPI DEV ENA N

[SPARES USED TO SIMULATE]

RCB	PCIe2VPX3UX4	Signal Name
A9	16	SPI CLK P
B9	50	SPI CLK N
D9	15	MOSI P
E9	49	MOSI N
B10	14	MISO P

C10	48	MISO N
E10	13	SPI DEV SEL 0 P
F10	47	SPI DEV SEL 1 N
A11	12	SPI DEV SEL 1 P
B11	46	SPI DEV SEL 1 N
D11	11	SPI DEV SEL 2 P
E11	45	SPI DEV SEL 2 N
B12	10	SPI DEV ENA P
C12	44	SPI DEV ENA N

Bezel High Density 69 pin connector

Name			Pin		
		OPN			2
OPN	OPN	GND	49	25	1
FAN3TACH	OPN	-15V	48	26	4
FAN2TACH	FANRTN	+5V	51	27	3
FAN1TACH	+12V	+7V	50	28	6
FAN0TACH	GND	+16V	53	29	5
OPN	+15V	OPN	52	30	8
ANTSEL2M	OPN	RS485RCVFPM	55	31	7
ANTSEL2P	ANTSEL0M	RS485RCVFPP	54	32	10
ANTSEL1M	ANTSEL0P	RS485XMITFPM	57	33	9
ANTSEL1P	ANTARYSELM	RS485XMITFPP	56	34	12
OPN	ANTARYSELP	OPN	59	35	11
CALSWB	OPN	GND	58	36	14
CALSRC2NDLOLCK	CLKTOCALSRC	CALSRCSELN	61	37	13
CALSRC1STLOLCK	MISOFRMCALSRC	CALSRCSELN0	60	38	16
OPN	MOSITOCALSRC	OPN	63	39	15
CALSWA	OPN	GND	62	40	18
AGND	OPN	RCVR2NDLOLCKN	65	41	17
ATTN7	AGND	RCVR1STLOLCKN	64	42	20
ATTN6	ATTN3	CLKTORCVRLO	67	43	19
AGND	ATTN2	MISOFRMRCVRLO	66	44	22
ATTN5	AGND	MOSITORCVRLO	69	45	21
ATTN4	ATTN1	RCVRLOSELN1	68	46	24
	ATTN0	RCVRLOSELN0		47	23

FIGURE 2 VPX RCB J1 69 PIN ASSIGNMENT

The Pin chart is in the same relative order as the footprint for the connector. The cable side has three rows made up of the pins from the three double columns. Pins1-24, 25-47, 48-69 make up the three rows on the cable side.

OPN = Open
GND = digital ground
AGND = analog ground reference for Attenuation circuits.
Voltages are inputs for monitoring circuit.

The recommended mate for this connector is MWDM2L-69S-6K7-18M and is available from GlenAir.

VPX P2 Rear IO

Name	Diff Pair #	Pin [P2]
SPI CLK IN P	DP0	A1
SPI CLK IN N	DP0	B1
MOSI P	DP1	D1
MOSI N	DP1	E1
MISO P	DP2	B2
MISO N	DP2	C2
SPI DEV SEL 0 P	DP3	E2
SPI DEV SEL 0 N	DP3	F2
SPI DEV SEL 1 P	DP4	A3
SPI DEV SEL 1 N	DP4	B3
SPI DEV SEL 2 P	DP5	D3
SPI DEV SEL 2 N	DP5	E3
SPI DEV EN P	DP6	B4
SPI DEV EN N	DP6	C4
485TOANT P	DP7	E4
485TOANT N	DP7	F4
485FRMANT P	DP8	A5
485FRMANT N	DP8	B5
RCVR 1ST LO LOCKN P	DP9	D5
RCVR 1ST LO LOCKN N	DP9	E5
CAL SRC 1ST LO LOCKN P	DP10	D5
CAL SRC 1ST LO LOCKN N	DP10	E5
ATTN TO HOST P	DP11	E6
ATTN TO HOST N	DP11	F6
BLANK0 P	DP12	A7
BLANK0 N	DP12	B7
BLANK1 P	DP13	D7
BLANK1 N	DP13	E7
BLANK2 P	DP14	B8
BLANK2 N	DP14	C8
BLANK3 P	DP15	E8
BLANK3 N	DP15	F8
SPARE0 P	DP16	A9
SPARE0 N	DP16	B9
SPARE1 P	DP17	D9
SPARE1 N	DP17	E9
SPARE2 P	DP18	B10
SPARE2 N	DP18	C10
SPARE3 P	DP19	E10
SPARE3 N	DP19	F10
SPARE4 P	DP20	A11
SPARE4 N	DP20	B11
SPARE5 P	DP21	D11
SPARE5 N	DP21	E11
SPARE6 P	DP22	B12
SPARE6 N	DP22	C12
ONEPPSOUT P	DP23	E12
ONEPPSOUT N	DP23	F12
BLANK_0 P	DP24	A13
BLANK_0 N	DP24	B13

BLANK_1 P	DP25	D13
BLANK_1 N	DP25	E13
BLANK_2 P	DP26	B14
BLANK_2 N	DP26	C14
BLANK_3 P	DP27	E14
BLANK_3 N	DP27	F14
EXT10MHZ P	DP28	A15
EXT10MHZ N	DP28	B15
ONEPPSIN P	DP29	D15
ONEPPSIN N	DP29	E15
RS485XMIT P	DP30	B16
RS485XMIT N	DP30	C16
RS485RX P	DP31	E16
RS485RX N	DP31	F16

FIGURE 3 VPX RCB P2 PIN ASSIGNMENT

Names are relative to the VPX-RCB. DP0-23 are LVDS. RS485 signals are indicated in the name. Other signals are system defined and have board level options to handle the voltage range. Please refer to the headers section.

Front Panel Clock Interface Pin Assignment

Name	Pin [J5,6,7]
10 MHZ	center conductor

FIGURE 4 VPX RCB FP CLK J5,6,7 PIN ASSIGNMENT

J5,6 and 7 are SSMA connectors with 10 MHz available. The signals are driven with TTL levels.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
VPX-RCB is a 3U 4 HP card meant to be installed into a VPX chassis. VPX-RCB is fitted with guide pins which aide in alignment prior to mating the VPX connectors. The VPX connectors are blade style and make high quality connections with reasonable insertion pressure required.

Install with the power off. Be sure to properly install the card – the bezel should be fully seated on the chassis mounting rail.

It is recommended to use the handle lock to fully seat and lock the card into place.

Attach any cables to be used.

Start-up
A third party PCI device cataloging tool will be helpful to check that the VendorID and CardID are “seen” by the OS.

The VPX standard does not distribute a clock for PCIe reference. VPX-RCB has a local 100 MHz reference oscillator. The upstream device must use non spread-spectrum clocking since VPX-RCB has no way to become synchronized with a spread-spectrum clock.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the VPX Receiver Controller when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time.

Construction and Reliability

The VPX Receiver Controller is constructed out of 0.062 high temp ROHS compliant material. Gold has been used for plating rather than Tin for improved performance over time. “leaded or unleaded” components can be used along with solder choices. Dynamic Engineering can support both processes.

Surface mounted components are used. The connectors are through hole soldered for the cables and compression fit for the VPX.

Thermal Considerations

The VPX Receiver Controller is built with “commercial” parts. The parts can be upgraded to provide an Extended Temperature “ET” version of the design. The connectors and other components are ET rated in either case.

The base design is fairly low powered and will not require a lot of cooling. External draw on the power supplies or IO signals can add a significant power load on the Receiver Controller. Forced air cooling is recommended in this case.

During T&I it is recommended to read the temperature sensor and see what temperature is registering on the board. If anywhere close to 70C forced air should be implemented. The MTBF will be longer at cooler temperatures [up to a point]. Remember that the LM81 is measuring the temperature on the FAB near the Bezel. Other parts may be warmer and likely are hotter than the surface temperature of the PCB. Getting the temperature reading below 50C would provide quite a bit of margin and add to the MTBF. If this is not possible the ET version is recommended as that adds 15C to the top end.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $150. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
InterNet Address support@dyneng.com

Specifications

Logic Interfaces:	PCIe Interface 4 lane Gen 1 and SPI
Access types:	PCIe target accesses. DMA can be added.
CLK rates supported:	10 MHz from rear panel or local osc, 10 MHz [LVTTL] on SSMA(3)
Power	local supplies for internal requirements based on +5, 3.3 and 12 from VPX bus.
SPI	Internal SPI used directly or converted to SMB. Registers are dual accessible from SPI and PCIe. Note some features are PCIe only.
IO	Additional miscellaneous and program specific IO are supported with a combination of RS-485, LVTTL, and LVDS.
D/A	8 channels of D/A are supported. Each channel is separately programmable. The output is buffered with an inverting opamp to provide a 0-M3.3V range. Register based programming with conversion status. Multi and single channel access.
Monitor	Two LM81's are supplied along with an SMB interface to measure the temperature, the local voltages and various external voltages.
DipSwitch	8 position switch supplied with register access. Switch can be used to differentiate between boards when more than one Receiver Controller is in the same system or for SW defined purposes.
FLASH	FPGA program is stored into FLASH memory with a JTAG header to allow for field updates and new programs.
Revision	The FPGA VHDL revision is programmed into a register to allow for SW detection of different revisions. When the base design changes a new CardID will be assigned.

Software Interface:	register mapped IO
Initialization:	registers are initialized to 0.
Interface:	Registers are R/W with the exception of Status bits.
Dimensions:	3U 4HP
Construction:	High Temp ROHS compliant Multi-Layer Printed Circuit board, Through Hole and Surface Mount Components. Standard processing with leaded components and solder. –ROHS option for ROHS compliant components and solder.

Order Information

extended temperature range –40 ⇔ +85C	
VPX-RCB	3U 4HP VPX card D/A, Temperature, Voltage Monitor, Fan Monitor High voltage “blanking” interface, SPI and PCIe control, Clock references, Extended Temp and Conformal Coating are standard on this model http://www.dyneng.com/VPX-RCB.html
-ROHS	Add for ROHS processing.