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PMC-Biserial-III NASA1 Base & Channels

Driver Documentation

Win32 Driver Model

Manual Revision A
Corresponding Hardware: Revision D
10-2005-0204
Corresponding Firmware:
NASA1: Design C, Revision 1

NASA1Base & NASA1Chan
WDM Device Drivers for the
PMC-Biserial-III-NASA1

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Introduction

The NASA1Base and NASA1Chan drivers are Win32 driver model (WDM) device drivers for the PmcBis3NASA1 from Dynamic Engineering.

The NASA1 driver package has two parts. The driver is installed into the Windows® OS, and the User Application "Userap" executable.

The driver is delivered as installed or executable items to be used directly or indirectly by the user. The Userap code is delivered in source form [C] and is for the purpose of providing a reference to using the driver.

UserAp is a stand-alone code set with a simple, and powerful menu plus a series of "tests" that can be run on the installed hardware. Each of the tests execute calls to the driver, pass parameters and structures, and get results back. With the sequence of calls demonstrated, the functions of the hardware are utilized for loop-back testing. The software is used for manufacturing test at Dynamic Engineering. For example most Dynamic Engineering PCI based designs support DMA. DMA is demonstrated with the memory based loop-back tests. The tests can be ported and modified to fit your requirements.

The test software can be ported to your application to provide a running start. It is recommended to port the switch and status tests to your application to get started. The tests are simple and will quickly demonstrate the end-to-end operation of your application making calls to the driver and interacting with the hardware.

The menu allows the user to add tests, to run sequences of tests, to run until a failure occurs and stop or to continue, to program a set number of loops to execute and more. The user can add tests to the provided test suite to try out application ideas before committing to your system configuration. In many cases the test configuration will allow faster debugging in a more controlled environment before integrating with the rest of the system.

The hardware has features common to the board level and features that are set apart in "channels". The channels have the same offsets within the channel, and the same status and control bit locations allowing for symmetrical software in the calling routines. The driver supports the channels with a variable passed in to identify which channel is being accessed. The hardware manual defines the pinout for each channel and the bitmaps and detailed configurations for each channel. The driver handles all aspects of interacting with the channels and base features. In some cases separate structures are used for different channels with specific channel based control bits passed. For example the UART channel has specific parameters for Parity control.

We strive to make a useable product, and while we can guarantee operation we can't

foresee all concepts for client implementation. If you have suggestions for extended features, special calls for particular set-ups or whatever please share them with us, [engineering@dyneng.com] and we will consider and in many cases add them.

The PmcBis3NASA1 design has a Spartan3 Xilinx FPGA to implement the PCI interface, FIFO's and protocol control and status for the IO. The IO are grouped into four channel's. Transmission and Reception can be accomplished with each channel under software control. Please refer to the HW manual for a much more complete description of the HW features.

A basic summary of base and channel board level features:

Base	PLL, Parallel Port, Switch, FLASH Revision, Design Revision
Channel 0	LLST interface
Channel 1	NMS Interface
Channel 2	UART Interface
Channel 3	Manchester Uplink & Downlink Interfaces

When the PmcBis3NASA1 board is recognized by the PCI bus configuration utility it will start the NASA1Base driver which will create a device object for each board, initialize the hardware, create a child devices for the channel(s) and request loading of the NASA1Chan driver. The NASA1Chan driver will create a device object for the I/O channel(s) and perform initialization on the channel(s). IO Control calls (IOCTLs) are used to configure the board and read status. Read and Write calls are used to move blocks of data in and out of the device.

Note:

This documentation will provide information about all calls made to the drivers, and how the drivers interact with the device for each of these calls. For more detailed information on the hardware implementation, refer to the PmcBis3NASA1 user manual (also referred to as the hardware manual).

Driver Installation

There are several files provided in each driver package. These files include driver: NASA1Base.sys, PmcBis3NASA1.inf, DDNASA1Base.h, NASA1BaseGUID.h, NASA1Chan.sys, DDNASA1Chan.h, NASA1ChanGUID.h. Userap: User Application source files.

NASA1BaseGUID.h and NASA1ChanGUID.h are C header files that define the device interface identifiers for the drivers. DDNASA1Base.h and DDNASA1Chan.h files are C header files that define the Application Program Interface (API) to the drivers. These files are required at compile time by any application that wishes to interface with the drivers, but they are not needed for driver installation. The files are included with the Userap fileset.

Windows 2000 Installation

Copy PmcBis3NASA1.inf, NASA1Base.sys and NASA1Chan.sys to a floppy disk, or CD if preferred. In some cases the files can be accessed over a network or from local HDD. Substitute the network address for the floppy instructions to proceed with an over the network installation. The files are stored at the root of the PmcBis3NASA1Userap file set.

With the hardware installed, power-on the PCI host computer and wait for the ***Found New Hardware Wizard*** dialogue window to appear.
_ Select ***Next***.
_ Select ***Search for a suitable driver for my device.***
_ Select ***Next***.
_ Insert the disk prepared above in the desired drive.
_ Select the appropriate drive e.g. ***Floppy disk drives***.
_ Select ***Next***.
_ The wizard should find the PmcBis3NASA1.inf file.
_ Select ***Next***.
_ Select ***Finish*** to close the ***Found New Hardware Wizard***.
The system should now see the channels and reopen the ***New Hardware Wizard.***
Repeat this for each channel as necessary.

Windows XP Installation

Copy PmcBis3NASA1.inf, NASA1Base.sys and NASA1Chan.sys to a floppy disk, or CD if preferred. In some cases the files can be accessed over a network or from local HDD. Substitute the network address for the floppy instructions to proceed with an over the network installation.

With the hardware installed, power-on the PCI host computer and wait for the ***Found New Hardware Wizard*** dialogue window to appear.
_ Insert the disk prepared above in the desired drive.
_ Select ***No when asked to connect to Windows Update***.
_ Select ***Next***.
_ Select ***Install the software automatically.***
_ Select ***Next***.
_ Select ***Finish*** to close the ***Found New Hardware Wizard***.
The system should now see the channels and reopen the ***New Hardware Wizard.***
Proceed as above for each channel as necessary.

Driver Startup

Once the drivers have been installed they will start automatically when the system recognizes the hardware. In many systems the drivers are associated with the slot the hardware is installed into. If you move slot positions you may need to reinstall the driver,

Handles can be opened to a specific board by using the CreateFile() function call and passing in the device names obtained from the system.

The interfaces to the devices are identified using globally unique identifiers (GUIDs), which are defined in NASA1BaseGUID.h and NASA1ChanGUID.h.

The User Application software contains a file called “main.c”. Main has the initialization needed to get the handles to the base and channel assets of the installed PmcBis3NASA1 device.

The main file provided is designed to work with our test menu and includes user interaction steps to allow the user to select which board is being tested in a multiple board environment. The integrator can hardcode for single board systems or use an automatic loop to operate in multiple board systems without using user interaction. For multiple user systems it is suggested that the board number is associated with a switch setting so the calls can be associated with a particular board from a physical point of view. The DIPswitch is provided for this purpose.

IO Controls

The drivers use IO Control calls (IOCTLs) to configure the device. IOCTLs refer to a single Device Object, which controls a single board or I/O channel. IOCTLs are called using the Win32 function DeviceIoControl() (see below), and passing in the handle to the device opened with CreateFile() (see above). IOCTLs generally have input parameters, output parameters, or both. Often a custom structure is used.

```
BOOL DeviceIoControl(
  HANDLE        hDevice,              // Handle opened with
                                      CreateFile()
  DWORD         dwIoControlCode,      // Control code defined in
                                      API header file
  LPVOID        lpInBuffer,           // Pointer to input parameter
  DWORD         nInBufferSize,        // Size of input parameter
  LPVOID        lpOutBuffer,          // Pointer to output
                                      parameter
  DWORD         nOutBufferSize,       // Size of output parameter
  LPDWORD       lpBytesReturned,      // Pointer to return length
                                      parameter
  LPOVERLAPPED  lpOverlapped,         // Optional pointer to
                                      overlapped structure
);                                    // used for asynchronous I/O
```

The IOCTLs defined for the NASA1Base driver are described below:
Please note that the address map is included in the DD file for reference when writing your own driver for a different OS.

IOCTL_NASA1_BASE_GET_INFO
Function: Return the Instance Number, Switch value, PLL device ID, Xilinx rev and Current Driver Version
Input: None
Output: NASA1_BASE_DRIVER_DEVICE_INFO : Structure
Notes: Switch value is the configuration of the on-board dip-switch that has been set by the User (see the board silk screen for bit position and polarity). The PLL ID is the device address of the PLL device. This value, which is set at the factory, is usually 0x69 but may also be 0x6A. See DDNASA1Base.h for the definition of NASA1_BASE_DRIVER_DEVICE_INFO.

IOCTL_NASA1_BASE_LOAD_PLL_DATA
Function: Loads the internal registers of the PLL.
Input: NASA1_BASE_PLL_DATA structure
Output: None
Notes:

IOCTL_NASA1_BASE_READ_PLL_DATA
Function: Returns the contents of the PLL's internal registers
Input: None
Output: NASA1_BASE_PLL_DATA structure
Notes: The register data is output in the NASA1_BASE_PLL_DATA structure in an array of 40 bytes.

IOCTL_NASA1_BASE_SET_BASEREG
Function: Write to Base Control Register - general access to base control register of card, use with bit definitions
Input: ULONG
Output: none
Notes: Use for general purpose – bit mapped access to the base control register.

IOCTL_NASA1_BASE_GET_BASEREG
Function: Read from Base Control Register - general access from base control register of card, use with bit definitions
Input: none
Output: ULONG
Notes: Use for general purpose – bit mapped access to the base control register.

IOCTL_NASA1_BASE_GET_STATUS
Function: Read from Status Register
Input: none
Output: ULONG
Notes: Use for general purpose – bit mapped access from the register. See DDNASA1Base.h for bit map information. See the HW manual for exact definitions of bits.

IOCTL_NASA1_BASE_SET_PARALLEL_DIR
Function: Write to Parallel Port Direction Register.
Input: ULONG
Output: none
Notes: D13-0 bits control Parallel Port bits 13-0. Set to transmit, clear to receive. Termination automatically adjusts to be enabled on receiving bits and disabled on transmitting bits.

IOCTL_NASA1_BASE_GET_PARALLEL_DIR
Function: Read-back from Parallel Port Direction Register.
Input: none
Output: ULONG
Notes:

IOCTL_NASA1_BASE_SET_PARALLEL_DATA
Function: Write to Parallel Port Data Register.
Input: ULONG
Output: none
Notes: D13-0 bits control Parallel Port bits 13-0. If set to transmit in [DIR register] the Data register bits are output as defined in this [Data] register.

IOCTL_NASA1_BASE_GET_PARALLEL_DATA
Function: Read-back from IO lines directly
Input: none
Output: ULONG
Notes: The IO levels may or may not match the output data since some of the lines may not be enabled to transmit or there may be external devices affecting the levels.

IOCTL_NASA1_BASE_GET_PARALLEL_DATA_REG
Function: Read-back from Data Definition register
Input: none
Output: ULONG
Notes: Direct read-back from the data definition register, will always match the data definition independent of direction register programming.

The IOCTLs defined for the NASA1Chan driver are described below:
In the NASA1 implementation both the Transmitter and the Receiver interface are implemented within the same channel (0,1,2,3). The Receiver accepts data from the external equipment. The Transmitter provides data to the external equipment. Loop-back can be accomplished with each channel looped to itself.

Address and bit map information is included in the DDNASA1Chan.h file to support those who are writing drivers for other OS.

IOCTL_NASA1_CHAN_GET_INFO
Function: Return the Instance Number and Current Driver Version
Input: None
Output: NASA1_CHAN_DRIVER_DEVICE_INFO structure
Notes: See the definition of NASA1_CHAN_DRIVER_DEVICE_INFO in the DDNASA1Chan.h header file.

IOCTL_NASA1_CHAN_GET_STATUS
Function: Return the value of the status register and clear latched bits
Input: None
Output: Status register value(ULONG)
Notes: Latched interrupt and error status are cleared by write-back. Defines available in DDNASA1Chan.h Detailed definitions are available in the HW manual. Several of the defines have different meanings depending on the channel being accessed. The .h file has the base definitions followed by specific definitions for the UART and Manchester interfaces [for the bits with alternate definitions].

IOCTL_NASA1_CHAN_CLR_STATUS
Function: Clear Error Bits latched and not cleared by status read
Input: ULONG
Output: none
Notes: Clear latched error bits. Allows polling on FIFO status without losing potential Error conditions. Write back with same bit position set to clear. Defines available in DDNASA1Chan.h Detailed definitions are available in the HW manual.

IOCTL_NASA1_CHAN_SET_FIFO_LEVELS
Function: Sets the transmitter almost empty and receiver almost full levels for the channel.
Input: NASA1_CHAN_FIFO_LEVELS structure
Output: None
Notes: The FIFO counts are compared to these levels to determine the value of the STAT_TX_FF_AE and STAT_RX_FF_AF status bits.

IOCTL_NASA1_CHAN_GET_FIFO_LEVELS
Function: Returns the transmitter almost empty and receiver almost full levels for the channel.
Input: None
Output: NASA1_CHAN_FIFO_LEVELS structure
Notes:

IOCTL_NASA1_CHAN_GET_FIFO_COUNTS
Function: Returns the number of data words in FIFO's.
Input: None
Output: NASA1_CHAN_FIFO_COUNTS structure
Notes: Returns the actual TX FIFO data counts and count including DMA pipeline RX FIFO, plus external and state machine FIFO levels if implemented.

IOCTL_NASA1_CHAN_RESET_FIFOS
Function: Resets one or all FIFO's for the referenced channel.
Input: NASA1_FIFO_SEL enumeration type See structure definition in DDNASA1Chan.h
Output: None
Notes: Resets Transmit, Receive, External or All FIFO's. Please note the Tx / Rx state machines are also reset by this command.

IOCTL_NASA1_CHAN_REGISTER_EVENT

Function: Registers an event to be signaled when an interrupt occurs.
Input: Handle to the Event object
Output: None
Notes: The caller creates an event with CreateEvent() and supplies the handle returned from that call as the input to this IOCTL. The driver then obtains a system pointer to the event and signals the event when a user interrupt is serviced. The user interrupt service routine waits on this event, allowing it to respond to the interrupt. The DMA interrupts do not cause the event to be signaled.

IOCTL_NASA1_CHAN_ENABLE_INTERRUPT

Function: Enables the channel Master Interrupt.
Input: None
Output: None
Notes: This command must be run to allow the board to respond to user interrupts. The master interrupt enable is disabled in the driver interrupt service routine when a user interrupt is serviced. Therefore this command must be run after each interrupt occurs to re-enable it.

IOCTL_NASA1_CHAN_DISABLE_INTERRUPT

Function: Disables the channel Master Interrupt.
Input: None
Output: None
Notes: This call is used when user interrupt processing is no longer desired.

IOCTL_NASA1_CHAN_FORCE_INTERRUPT

Function: Causes a system interrupt to occur.
Input: None
Output: None
Notes: Causes an interrupt to be asserted on the PCI bus as long as the channel master interrupt is enabled. This IOCTL is used for development, to test interrupt processing. Board level master interrupt also needs to be set.

IOCTL_NASA1_CHAN_GET_ISR_STATUS

Function: Returns the interrupt status read in the ISR from the last user interrupt.
Input: None
Output: Interrupt status value (unsigned long integer)
Notes: Returns the interrupt status that was read in the interrupt service routine of the last interrupt caused by one of the enabled channel interrupts. The interrupts that deal with the DMA transfers do not affect this value. Masked version of channel status.

IOCTL_NASA1_CHAN_SWW_TX_FIFO
Function: Writes a 32-bit data word to the transmit FIFO.
Input: FIFO word (unsigned long integer)
Output: none
Notes: Used to make single-word accesses to the transmit FIFO instead of using DMA.

IOCTL_NASA1_CHAN_SWR_RX_FIFO
Function: Returns a 32-bit data word from the receive FIFO.
Input: None
Output: FIFO word (unsigned long integer)
Notes: Used to make single-word accesses to the receive FIFO instead of using DMA. Please note, Data read from this port is no longer available in the FIFO for DMA or other use.

IOCTL_NASA1_CHAN_SET_CONTROL
Function: write to Channel Control register using structure
Input: NASA1_CHAN_CONT
Output: None
Notes: See DDNASA1Chan.h for structure. Some Channel Control functions are specific to a particular channel. The HW manual has detailed information on the function of each option and which channels are able to use that option.

IOCTL_NASA1_CHAN_GET_CONTROL
Function: Read from Channel Control register using structure
Input: None
Output: NASA1_CHAN_CONT
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_SET_TX
Function: write to Channel Tx Control register using structure
Input: NASA1_CHAN_TX_CONTROL
Output: None
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_GET_TX
Function: Read from Channel TX Control register using structure
Input: None
Output: NASA1_CHAN_TX_CONTROL
Notes: See DDNASA1Chan.h for structure.

Please note: UART and Uplink have separate calls and structures.

IOCTL_NASA1_CHAN_SET_TX_UART
Function: write to Channel Tx Control register using structure specific to UART control
Input: NASA1_CHAN_TX_CONTROL_UART
Output: None
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_GET_TX_UART
Function: Read from UART channel TX control register using structure
Input: None
Output: NASA1_CHAN_TX_CONTROL_UART
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_SET_UPLINK
Function: write to Channel Tx Control register using structure specific to Uplink control
Input: NASA1_CHAN_UPLINK_CONTROL
Output: None
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_GET_UPLINK
Function: Read from Channel Tx Control register using structure
Input: None
Output: NASA1_CHAN_UPLINK_CONTROL
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_SET_TX_COUNT
Function: write to Channel TXCount register
Input: ULONG
Output: None
Notes: D31-D30 = Bytes to use, D29-0 = number of LW to send including last [potentially] partial word

IOCTL_NASA1_CHAN_GET_TX_COUNT
Function: Read from Channel TX Count Register
Input: None
Output: ULONG
Notes:

IOCTL_NASA1_CHAN_SET_TX_READY
Function: write to Channel TX Ready Count Register
Input: ULONG
Output: None
Notes: Set the count for starting the Transmitter. When the transmitter is enabled the State-machine waits for the READY COUNT level matched against the total FIFO path for TX .

IOCTL_NASA1_CHAN_GET_TX_READY
Function: Read from Channel TX Ready Count Register
Input: None
Output: ULONG
Notes: Read back port.

IOCTL_NASA1_CHAN_SET_TX_AMT
Function: write to Channel TX Almost Empty Count Register
Input: ULONG
Output: None
Notes: Set the count for comparing against the TX FIFO path total count for the Almost Empty condition. The Almost Empty level interrupt control count is set with this register.

IOCTL_NASA1_CHAN_GET_TX_AMT
Function: Read from Channel TX Almost Empty Count Register
Input: None
Output: ULONG
Notes: Read back port.

IOCTL_NASA1_CHAN_TX_FIFO_WORDCNT_READ
Function: Read Level of Data stored in Transmit Local FIFO
Input: None
Output: ULONG
Notes: Read only. 1Kx32 max value. Unused NASA1.

IOCTL_NASA1_CHAN_EXT_FIFO_WORDCNT_READ
Function: Read Level of Data stored in External FIFO
Input: None
Output: ULONG
Notes: Read only. 128Kx32 max value. Please note the External FIFO is used for both RX and TX functions. Unused NASA1

IOCTL_NASA1_CHAN_TX_FIFO_TOTALWORDCNT_READ
Function: Read Combined Level of Data stored in DMA, External and TX SM FIFO's
Input: None
Output: ULONG
Notes: Read only. 133Kx32 max value. Please note that values in the External FIFO will show in this count even if channel is set to RX mode. Unused NASA1

IOCTL_NASA1_CHAN_SET_RX
Function: write to Channel Receiver Control register using structure
Input: NASA1_CHAN_RX_CONTROL
Output: None
Notes: See DDNASA1Chan.h for structure. See HW manual for more detail on individual bit control. Valid for LLST and NMS. See separate UART and Downlink commands.

IOCTL_NASA1_CHAN_GET_RX
Function: Read from Channel Receiver Control register using structure
Input: None
Output: NASA1_CHAN_RX_CONTROL
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_SET_RX_UART
Function: write to Channel Receiver Control register using structure
Input: NASA1_CHAN_RX_CONTROL_UART
Output: None
Notes: See DDNASA1Chan.h for structure. See HW manual for more detail on individual bit control. Valid for UART channel.

IOCTL_NASA1_CHAN_GET_RX_UART
Function: Read from Channel Receiver Control register using structure
Input: None
Output: NASA1_CHAN_RX_CONTROL_UART
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_SET_DOWNLINK
Function: write to Channel Receiver Control register using structure
Input: NASA1_CHAN_DOWNLINK_CONTROL
Output: None
Notes: See DDNASA1Chan.h for structure. See HW manual for more detail on individual bit control. Valid for Downlink commands.

IOCTL_NASA1_CHAN_GET_DOWNLINK
Function: Read from Channel Receiver Control register using structure
Input: None
Output: NASA1_CHAN_DOWNLINK_CONTROL
Notes: See DDNASA1Chan.h for structure.

IOCTL_NASA1_CHAN_SET_RX_COUNT
Function: write to Channel Receiver Count register
Input: ULONG
Output: None
Notes: Set the count for the size of the packet to be received. Unused NASA1 channels LLST, NMS, UART. Alternate use for Downlink – Synchronization Pattern. Coordinate bytes used for synchronization pattern with bytes enabled with DOWNLINK control register for synchronization. D31 used for Static mode operation. See HW manual for more detail.

IOCTL_NASA1_CHAN_GET_RX_COUNT
Function: Read from Channel Receiver Count register
Input: None
Output: ULONG
Notes: Unused NASA1 channels LLST, NMS, UART. Alternate use for Downlink Read-back synchronization pattern.

IOCTL_NASA1_CHAN_SET_RX_AFL
Function: write to Channel Receiver Almost Full Register
Input: ULONG
Output: None
Notes: Set the level to compare against for the Almost Full Level interrupt. The level is compared against the total RX FIFO path data and when the FIFO path has more data than the AFL register value the AFL interrupt and status are set.

IOCTL_NASA1_CHAN_GET_RX_AFL
Function: Read from Channel Receiver Almost Full Register
Input: None
Output: ULONG
Notes:

IOCTL_NASA1_CHAN_RX_FIFO_TOTALWORDCNT_READ
Function: Read Combined Level of Data stored in DMA Pipeline, RX DMA, External and RX SM FIFO's
Input: None
Output: ULONG
Notes: Read only. Unused NASA1 133Kx32 max value. Please note that values in the External FIFO will show in this count even if channel is set to TX mode. This count can be used to set "final" DMA read values when reception is stopped and the image count is not known.

Write

DMA data is written to the referenced I/O channel device using the write command. Writes are executed using the Win32 function WriteFile() and passing in the handle to the I/O channel device opened with CreateFile(), a pointer to a pre-allocated buffer containing the data to be written, an unsigned long integer that represents the size of that buffer in bytes, a pointer to an unsigned long integer to contain the number of bytes actually written, and a pointer to an optional Overlapped structure for performing asynchronous IO.

Read

DMA data is read from the referenced I/O channel device using the read command. Reads are executed using the Win32 function ReadFile() and passing in the handle to the I/O channel device opened with CreateFile(), a pointer to a pre-allocated buffer that will contain the data read, an unsigned long integer that represents the size of that buffer in bytes, a pointer to an unsigned long integer to contain the number of bytes actually read, and a pointer to an optional Overlapped structure for performing asynchronous IO.

Examples of using DMA are provided in the reference software FIFO and IO loop-tests.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering’s products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the driver is at fault. The driver has gone through extensive testing and in most cases it will be “cockpit error” rather than an error with the driver. When you are sure or at least willing to pay to have someone help then call the Customer Service Department and arrange to speak with an engineer. We will work with you to determine the cause of the issue. If the issue is one of a defective driver we will correct the problem and provide an updated module(s) to you [no cost]. If the issue is of the customer’s making [anything that is not the driver] the engineering time will be invoiced to the customer. Pre-approval may be required in some cases depending on the customer’s invoicing policy.

Out of Warranty Repairs

Out of warranty support will be billed. The current minimum repair charge is $125. An open PO will be required.

For Service Contact:

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Appendix

Reference copy of structures for evaluation

The following structures shown are available in the DDNASA1Chan.h and DDNASA1Base.h files included with the driver. The structures are included here for your evaluation when considering the driver package. The electronic versions included with the driver should be used with your project. The names track the register bit definitions. For details about particular signals please refer to the HW manual.

Base:

```
#define PLL_MESSAGE1_SIZE       16
#define PLL_MESSAGE2_SIZE       24
#define PLL_MESSAGE_SIZE        (PLL_MESSAGE1_SIZE + PLL_MESSAGE2_SIZE)

 // Driver/Device information
typedef struct _NASA1_BASE_DRIVER_DEVICE_INFO
{
   UCHAR    DriverVersion;
   UCHAR    XilinxVersion;
   UCHAR    XilinxDesign;
   UCHAR    PllDeviceId;
   UCHAR    SwitchValue;
   ULONG    InstanceNumber;
} NASA1_BASE_DRIVER_DEVICE_INFO, *PNASA1_BASE_DRIVER_DEVICE_INFO;

typedef struct _NASA1_BASE_PLL_DATA
{
   UCHAR    Data[PLL_MESSAGE_SIZE];
} NASA1_BASE_PLL_DATA, *PNASA1_BASE_PLL_DATA;
```

Channel:

```
typedef struct _NASA1_CHAN_DRIVER_DEVICE_INFO
{
  UCHAR    DriverVersion;
  ULONG    InstanceNumber;
} NASA1_CHAN_DRIVER_DEVICE_INFO, *PNASA1_CHAN_DRIVER_DEVICE_INFO;

typedef enum _NASA1_CHAN_FIFO_SEL {NASA1_RX, NASA1_TX, NASA1_EXT,
NASA1_ALL} NASA1_CHAN_FIFO_SEL, *PNASA1_CHAN_FIFO_SEL;

typedef struct _NASA1_CHAN_FIFO_LEVELS
{
  USHORT   AlmostFull;              // Set to control Master HW with Almost full definition
  USHORT   AlmostEmpty;             // set to control Target HW with Almost Empty definition,
Also controls Interrupt request
} NASA1_CHAN_FIFO_LEVELS, *PNASA1_CHAN_FIFO_LEVELS;

typedef struct _NASA1_CHAN_FIFO_COUNTS
{
  USHORT            RxCountwPipe;       // RX DMA FIFO plus pipeline
  USHORT            TxCount;            // TX DMA FIFO
} NASA1_CHAN_FIFO_COUNTS, *PNASA1_CHAN_FIFO_COUNTS;

typedef struct _NASA1_CHAN_CONT
{
  BOOLEAN           FifoTestEn;         // BiPass Mode Control
  BOOLEAN           MIntEn;             // Master Interrupt Enable
  BOOLEAN           WrDmaEn;            // Write DMA Interrupt Enable
  BOOLEAN           RdDmaEn;            // Read DMA Interrupt Enable
  BOOLEAN           TxUrgent;           // Set for higher priority TX DMA processing
  BOOLEAN           RxUrgent;           // Set for higher priority RX DMA processing
  USHORT            RateDiv;            // Set divisor for local clock selection.
} NASA1_CHAN_CONT, *PNASA1_CHAN_CONT;
```

```
typedef struct _NASA1_CHAN_RX_CONTROL
{
  BOOLEAN          RxStart;          //0 set to begin RX Data Acquisition
  BOOLEAN          RxIntEn;          //2 set to enable RX interrupt for each image
                                       captured
  BOOLEAN          RxAFIntEn;        //3 set to enable RX DMA FIFO based interrupt
                                       [almost full]
  BOOLEAN          RxOvFlEn;         //4 set to enable RX OverFlow interrupt
  BOOLEAN          RxByteOrder;      //5 set to reverse bytes after receiving
  BOOLEAN          RxAFIntEnLvl;     //6 set to enable Almost Full FIFO interrupt based
                                       on AF level.  Int active whenever AFull is true
  BOOLEAN          RxFifoPathEn;     //10 set to enable data movement from RX FIFO to
                                       Ext FIFO & from Ext FIFO to RX DMA FIFO
} NASA1_CHAN_RX_CONTROL, *PNASA1_CHAN_RX_CONTROL;


typedef struct _NASA1_CHAN_TX_CONTROL
{
  BOOLEAN          TxStart;          //0 start TX state machine
  BOOLEAN          TxFifoEn;         //1 set to begin enable data transfer from ext fifo to
                                       TX fifo
  BOOLEAN          TxIntEn;          //2 set to enable TX interrupt - occurs when each
                                       image is transmitted
  BOOLEAN          TxAEIntEn;        //3 set to enable TX FIFO based interrupt [almost
                                       empty] based on latched status (requires not
                                       almost empty to become almost mt
  BOOLEAN          TxUnFlEn;         //4 set to enable UnderFlow interrupt
  BOOLEAN          TxByteOrder;      //5 set to use upper [D31-16] then lower[D15-0],
                                       clear to use lower then upper
  BOOLEAN          TxAEIntEnLvl;     //6 set to enable Almost Empty FIFO interrupt
                                       based on AE level.  Interrupt active whenever
                                       almost empty is true
} NASA1_CHAN_TX_CONTROL, *PNASA1_CHAN_TX_CONTROL;
```

```
typedef struct _NASA1_CHAN_RX_CONTROL_UART
{
  BOOLEAN          RxStart;          //0 set to begin RX Data Acquisition
  BOOLEAN          RxIntEn;          //2 set to enable RX interrupt for each packet
                                     captured
  BOOLEAN          RxAFIntEn;        //3 set to enable RX DMA FIFO based interrupt
                                     [almost full]
  BOOLEAN          RxOvFlEn;         //4 set to enable RX OverFlow interrupt
  BOOLEAN          RxByteOrder;      //5 set to reverse bytes after receiving
  BOOLEAN          RxAFIntEnLvl;     //6 set to enable Almost Full FIFO [total FIFO count]
                                     interrupt based on AF level.  Interrupt active
                                     whenever almost Full is true
  BOOLEAN          RxByteMode;       //7 set to select ByteMode, clear to select
                                     PacketMode
  BOOLEAN          RxParityEn;       //8 set to enable Parity
  BOOLEAN          RxParityOdd;      //9 set to Select Odd Parity, requires Parity to be
                                     enabled
  BOOLEAN          RxStop2;          //10 set to cause at least 2 stop / marking bits
                                     between bytes sent
} NASA1_CHAN_RX_CONTROL_UART, *PNASA1_CHAN_RX_CONTROL_UART;

typedef struct _NASA1_CHAN_TX_CONTROL_UART
{
  BOOLEAN          TxStart;          //0 start TX state machine
  BOOLEAN          TxStartClr;       //1 set to enable PacketComplete to clear TX
                                     Enable, autostop at end of packet sent
  BOOLEAN          TxIntEn;          //2 set to enable TX interrupt - occurs when each
                                     image is transmitted
  BOOLEAN          TxAEIntEn;        //3 set to enable TX FIFO based interrupt [almost
                                     empty] based on latched status (requires not
                                     almost empty to become almost mt
  BOOLEAN          TxUnFlEn;         //4 set to enable UnderFlow interrupt
  BOOLEAN          TxByteOrder;      //5 set to use upper [D31-16] then lower[D15-0],
                                     clear to use lower then upper
  BOOLEAN          TxAEIntEnLvl;     //6 set to enable Almost Empty FIFO interrupt
                                     based on AE level.  Interrupt active whenever
                                     almost empty is true
  BOOLEAN          TxByteMode;       //7 set to select ByteMode, clear to select
                                     PacketMode
  BOOLEAN          TxParityEn;       //8 set to enable Parity
  BOOLEAN          TxParityOdd;      //9 set to Select Odd Parity, requires Parity to be
                                     enabled
  BOOLEAN          TxStop2;          //10 set to cause at least 2 stop / marking bits
                                     between bytes sent
  BOOLEAN          TxClkSel;         //11 1 = push TX clock reference onto TX UART IO,
                                     0 = Normal
} NASA1_CHAN_TX_CONTROL_UART, *PNASA1_CHAN_TX_CONTROL_UART;
```

```
typedef struct _NASA1_CHAN_DOWNLINK_CONTROL
{
  BOOLEAN          RxStart;          //0 set to begin RX Data Acquisition
  BOOLEAN          RxIntEn;          //2 set to enable RX interrupt for each packet Rx'd
  BOOLEAN          RxAFIntEn;        //3 set to enable RX DMA FIFO based interrupt
                                     [almost full]
  BOOLEAN          RxOvFlEn;         //4 set to enable RX OverFlow interrupt
  BOOLEAN          RxByteOrder;      //5 set to reverse bytes after receiving
  BOOLEAN          RxAFIntEnLvl;     //6 set to enable Almost Full FIFO [total FIFO count]
                                     interrupt based on AF level.  Interrupt active
                                     whenever almost Full is true
  BOOLEAN          RxByteMode;       //7 set to select ByteMode, clear to select
                                     PacketMode
  BOOLEAN          RxSFwMode;        //8 set to select StaticMode, clear for FreeWheel
  BOOLEAN          RxDataPhase;      //10 (0) selects BiPhase-L, (1) selects data
                                     inversion for BiPhase-H
  USHORT           SyncSel;          //15-12 Enable Bytes for Sync detection (3-0) used
                                     in passed parameter
  BOOLEAN          RxReSync;         //31 (1) causes resync request, self cleared when
                                     new sync achieved
  USHORT           RateDiv;          // Set divisor for DownLink 8x clock selection
} NASA1_CHAN_DOWNLINK_CONTROL, *PNASA1_CHAN_DOWNLINK_CONTROL;

typedef struct _NASA1_CHAN_UPLINK_CONTROL
{
  BOOLEAN          TxStart;          //0 start TX state machine
  BOOLEAN          TxStartClr;       //1 set to enable PacketComplete to clear TX
                                     Enable, autostop at end of packet sent
  BOOLEAN          TxIntEn;          //2 set to enable TX interrupt - occurs when each
                                     packet  is transmitted
  BOOLEAN          TxAEIntEn;        //3 set to enable TX FIFO based interrupt [almost
                                     empty] based on latched status (requires not
                                     almost empty to become almost mt
  BOOLEAN          TxUnFlEn;         //4 set to enable UnderFlow interrupt
  BOOLEAN          TxByteOrder;      //5 set to use upper [D31-16] then lower[D15-0],
                                     clear to use lower then upper
  BOOLEAN          TxAEIntEnLvl;     //6 set to enable Almost Empty FIFO interrupt
                                     based on AE level.  Interrupt active whenever
                                     almost empty is true
  BOOLEAN          TxByteMode;       //7 set to select ByteMode, clear to select
                                     PacketMode
  BOOLEAN          TxSFwMode;        //8 set to select StaticMode, clear for FreeWheel
  BOOLEAN          TxStaticSelect;   //9 use '0' to select '0' or '1' to select last bit sent for
                                     static value
  BOOLEAN          TxDataPhase;      //10 (0) selects BiPhase-L, (1) selects data
                                     inversion for BiPhase-H
  USHORT           RateDiv;          // Set divisor for UpLink 2x clock selection
} NASA1_CHAN_UPLINK_CONTROL, *PNASA1_CHAN_UPLINK_CONTROL;
```