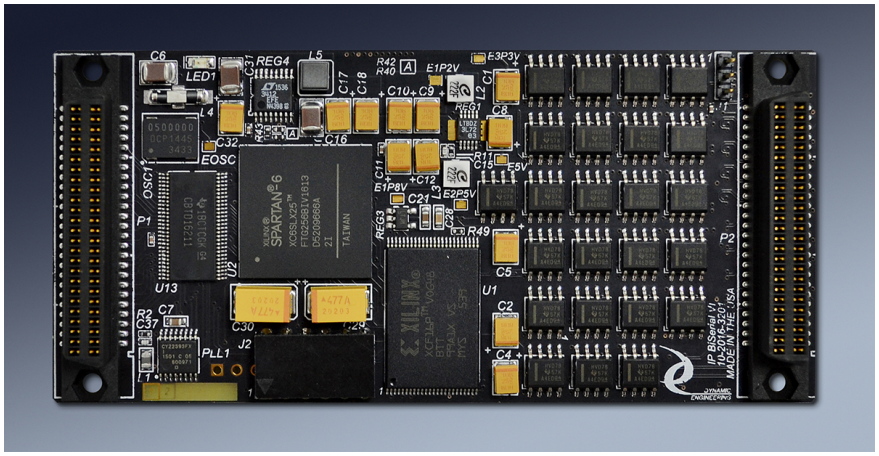
DYNAMIC ENGINEERING
150 DuBois St. Suite C Santa Cruz, CA 95060
831-457-8891 **Fax** 831-457-4793
sales@dyneng.com
www.dyneng.com
Est. 1988

User Manual

IP-BiSerial-VI-SIB

SDC/SDT or USIP/USOP Serial Interface

RS485
IndustryPack® Module



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Corresponding Hardware: Revision 01
FLASH revision: Std 0101 Fab: 10-2016-3201

IP-BiSerial-VI-SIB
SDC/SDT or USIP/USOP Serial Interface
IndustryPack® Module

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised January 30, 2017

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Product Description

IP-BiSerial-VI-SIB is implemented using IP-BiSerial-VI outfit with 24 RS-485 transceivers. The FLASH loaded manifests the SIB specification as described below.

IP-BiSerial-VI is part of the IndustryPack® "IP" Module family of I/O components by Dynamic Engineering. IP-BiSerial-VI provides an IP Module type II compliant mechanical package with a Spartan 6 FPGA, FLASH, PLL(4 reference clocks to FPGA), 24 differential IO [LVDS and/or RS485] each with separately programmable terminations and direction controls. The FLASH is easily reprogrammable with the Xilinx Impact SW and USB adapter – there is a header for this purpose.

The Differential IO are routed to the connector with controlled impedance, matched length [FPGA to IO pin pairs], and pin definitions consistent with the Dynamic Engineering standard for differential IO on IP Modules [1,2 … 23,24 (25,50 grounds), 26,27…48,49]. This definition is implemented on Dynamic Engineering Carrier designs supporting differential pairs [PCIe3IP, PCIe5IP, PCI3IP, PCI5IP, VPX2IP] to name a few.

SIB is designed with a two level hierarchy – Base and Channel. The Base level has the IP Bus interface and decoding, master interrupt control, PLL programming [unused], clock generation, and Channel instantiation. Each of the 2 channels has the same capabilities. SDC/SDT or USIP/USOP support with several programmable options discussed in the following paragraphs.

In SDC/SDT Mode the Clock and Gate are received, the data is transmitted by the SDT and received by the SDC portion of the interface. CTS is provided but not required for operation. Interrupt or polled operation.

In USIP/USOP Mode the Data, Clock, and Gate are transmitted by the USOP side of the channel and received by USIP. In addition USIP transmits CTS to indicate USOP can transmit data. The Clear To Send signal is deasserted when the Rx FIFO is almost full. The Transmitter detects the deassertion and stops at the next word boundary. This may happen 2 words after deassertion if the deassertion is near the end of a word. CTS can be inverted and disabled via the channel control register. CTS is normally asserted '1' when data can be transmitted, and '0' to hold off. With the CTSsense bit '0' can mean transmit and '1' hold off to match your system. When disabled the line is held in the hold off state based on the CTSsense definition.

The USOP transmit reference clock is 1 MHz, and is derived from the 50 MHz oscillator. The oscillator frequency is divided down to 2 MHz and distributed to the channels.

Within each channel the 2 MHz is divided to 1 MHz. IP-BiSerial-VI features 8 clockout/clock in pairs [IO connections between closely located pins where an IO is tied to a clock input pin]. This allows the divided signal to be brought back into the FPGA and treated as a clock [Channel Reference Clock]. This feature was borrowed from PMC-BiSerial-VI.

The receivers in both modes utilize a higher rate clock. The clock is used to sample the data, clock, and gate to determine when to capture data. In the SDC mode the clock is bursted. This approach allows for a parked clock without consequence.

Separate State Machines are utilized to operate transmit and receive functions allowing for independent operation. At this time the mode selection switches between SDC&SDT or USOP&USIP.

Status is available to allow polled or interrupt driven operation, amount of data in the FIFO's, State Machine Idle, state of CTS [Tx received], and Rx FIFO OverFlow.

Test capabilities are built in to support loop-back in the SDC/SDT mode. A gate and clock generator are part of the base of the design. The clock can be enabled or disabled via the base control register. Writing to the Gate Count register starts a transfer with 4 copies of the gate driven from the unused upper IO to support the 4 total inputs on the two channels.

Both modes transmit/receive 16 bit data, msb first, rising edge valid. The transmitters change outputs with the falling edge of the reference clock providing almost ½ period of setup/hold at the receiver.

For the following figures: Blue represents re-arming paths. Red for delay paths. Green for Advance paths. Black for return to IDLE. Return to Idle can happen if the Enable is disabled. It is recommended to return to the IDLE state when changing modes of operation.

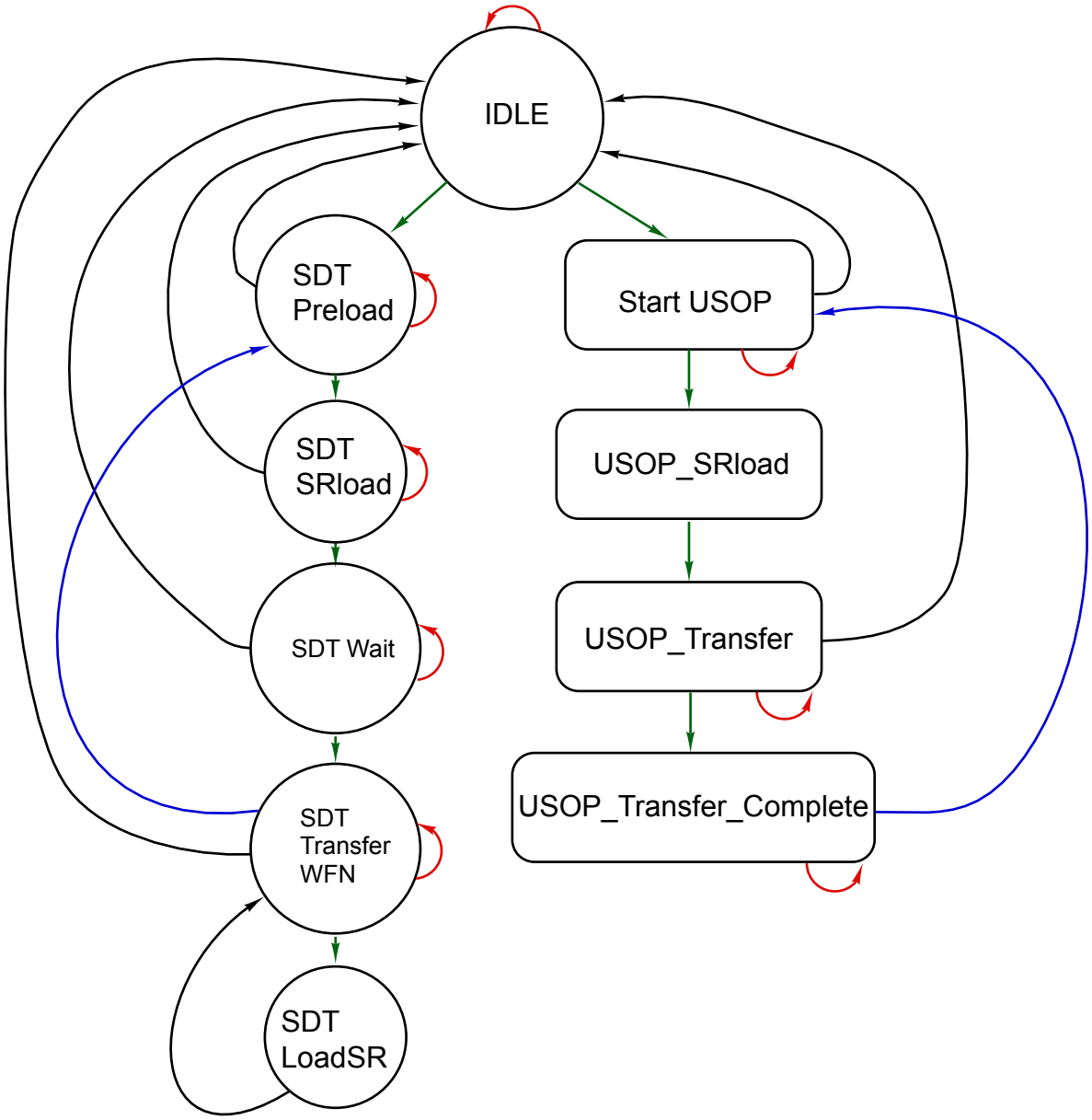

FIGURE 1 IP-BISERIAL-VI-SIB STATE TX FLOW DIAGRAM

The transmit function has two distinct modes: SDT and USOP. With SDT the Clock and Gate are received with the data transmitted [relative to the SIB]. The SDT Preload and SDT SRload states take care of making sure there is data in the FIFO and that the received Gate is in the non-active state. When proceding to the SDT Wait state, the shift register is preloaded with the next FIFO word. The received clock line is sampled to find the rising edge with Gate asserted. Once Gate has been detected to have

transitioned to an active state the clock is polled for the falling edge. With the falling edge data is transitioned or loaded as appropriate to provide the msb first serial data stream. This continues until Gate is invalid on a falling edge of the received clock. The state machine transitions back to the preload state to reinitialize. 16 bit data transfers [or multiples thereof] are expected. Any bits remaining in the last word are dumped with a non-x16 gate length.

USOP is a little different in that the Clock and Gate come from the transmitter and CTS is checked to hold off transfers. Start USOP Checks for CTS being valid to transmit, and FIFO has data. USOP_SRload loads the shift register for the first word transfer in each transmission. The transfer state tracks the data count and reloads when almost completed with each word to provide continuous data, CTS is monitored and if disabled the state machine will complete the current word possibly +1 and stop transmission. When CTS is disabled Gate will be disabled essentially breaking the transfer into two smaller transmissions. An interrupt is generated for each segment. Similarly if the FIFO becomes empty during the transmission, transmission will complete and the HW return to the start state waiting more data or an active CTS signal.

The receiver design is combined for both types since the same processing can be used for USIP and SDC. The 50 MHz clock is used to detect clock transitions and the gate signal monitored to know when data is valid. Data is captured on the rising edge of the clock and expected MSB first. CTS is generated for both modes. It is expected to only be used for the USOP function, but is available for SDT if desired. The Almost full condition for the FIFO is used to automatically assert CTS disabled when almost full. The Transmitter can send more data after CTS is transitioned to disabled and remaining locations in the FIFO will prevent an overflow.

Please note: over flow status is available in the channel status register. CTS can also be forced off and the sense changed through the control register.

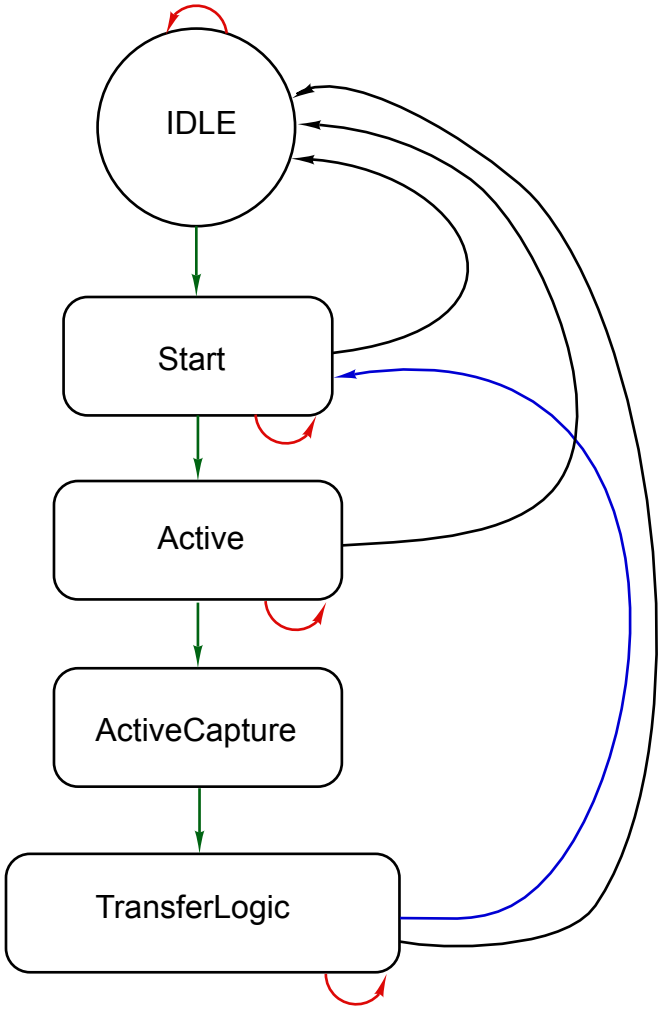

FIGURE 2 IP-BISERIAL-VI-SIB STATE RX FLOW DIAGRAM

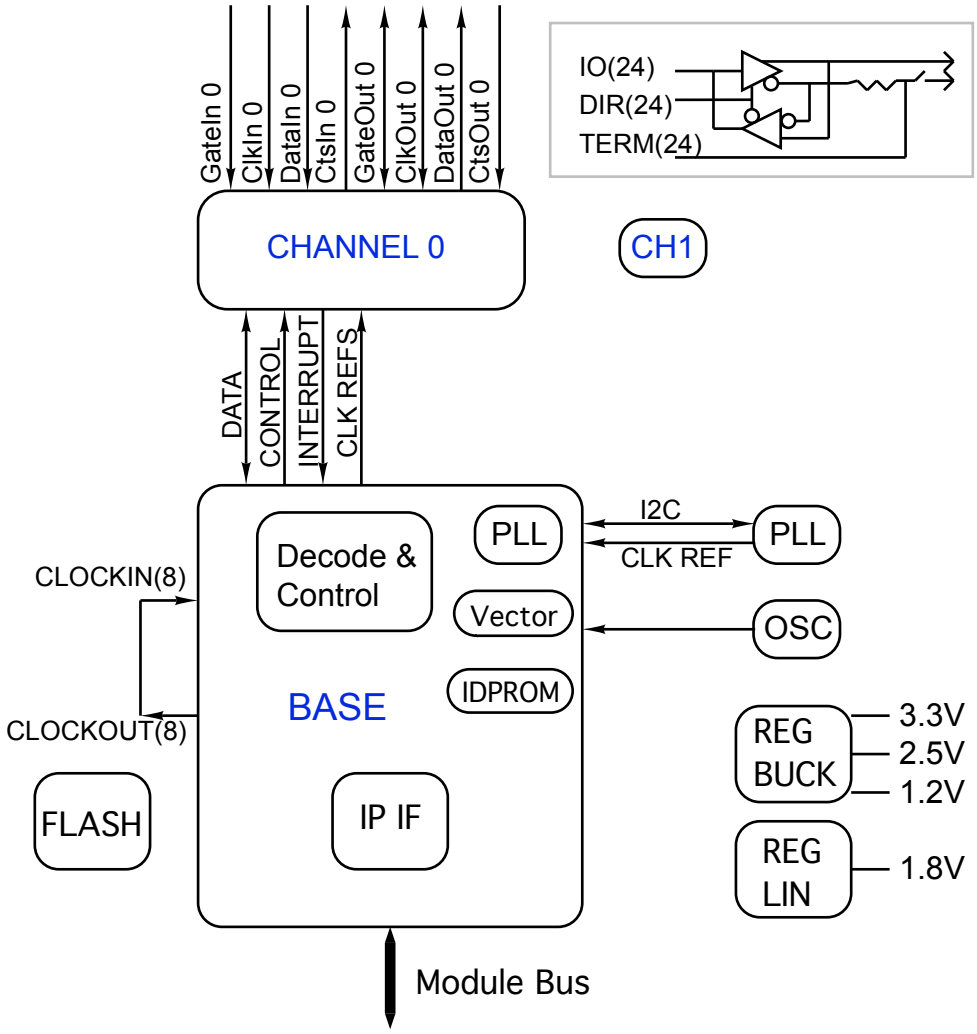

FIGURE 3 IP-BISERIAL-VI-SIB BLOCK DIAGRAM

IP-BiSerial-VI incorporates 24 differential pairs, each of which can be LVDS or RS485. For SIB, RS485 is implemented with each of the 2 channels using 8 of the IO. Each channel has inputs and outputs. Some signals can be inputs or outputs and are marked with bidirectional arrows in the diagram. The “In” signals are for the receiver port. The “Out” signals for the transmitter port. With the SDT mode the GateOut and ClkOut signals are received by the transmitter with the Data being transmitted. When USOP is selected the ClkOut and GateOut become outputs.

Within each channel are two state-machines as shown in Figures 1&2 plus the supporting logic for independent operation.

The Spartan VI requires three voltages, derived via Buck regulators from the 5V IP standard voltage [3.3V, 2.5V, and 1.2V]. In addition the FLASH requires a small amount of 1.8V and a linear regulator is provided for this purpose. The 3.3V rail is also used for the LVDS and RS-485 devices allowing mix and match assembly.

The PLL is provided but not used in the SIB Design. The installed oscillator is a 50 MHz model with 10 ppm. Additional board level clocking options include the ClockOut to ClockIn network. Each of the 8 ClockOut signals is tied back to a clock input on the FPGA allowing flexibility. This clock bus is used within SIB.

The FLASH is used to store the module firmware – in this case the SIB function.

The Base level of the design provides the IndustryPack interface, general decoding, card level status, IDPROM and Vector register plus board level features ⇔ PLL, interrupt masking, master channel enable.

Each Channel is the same in the case of SIB. The decoded data bus is routed to each channel along with decoded read and write controls to allow SW control over channel assets. Each channel has a control register, status register, Almost Full and Almost Empty definitions [FIFO's], and reference clock counter read-back.

Please refer the address/bit maps for details of the various registers and operation.

IP-BiSerial-VI-SIB conforms to the IndustryPack® standard. This guarantees compatibility with compliant carrier boards. Because the IP-BiSerial-VI-SIB may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCIe3IP – PCI carrier for IP Modules can be used for development in a conventional PC. Later the hardware and software can be ported to the target. http://www.dyneng.com/PCIe5IP.html

With the Dynamic Engineering Windows driver collection for IP and carrier modules a Parent – Child architecture is employed. The IP portion of the driver is directly portable between the various Dynamic Engineering IP carriers [PCIe3IP, PCI3IP, PCIe5IP, PCI5IP, PC104pIP, PC104p4IP, cPCI2IP, cPCI4IP etc]. The parent portion of the driver contains the carrier specific design information. This means that software developed for the IP-BiSerial-VI-SIB on one platform can be directly ported to another. PCI to cPCI for example.

Designers can make use of the Dynamic Engineering carrier driver for non-Dynamic Engineering IP modules using the Generic IP capability built into the parent portion of

the driver. IP modules that the carrier driver does not recognize are installed as “generic” and accessed with a address, data interface model. Software developed for the Generic mode can also be ported between modules.

IP-BiSerial-VI-SIB is tested with a combination of internal and external tests. The registers can be tested with R/W tests, the channels can be tested with the external loop-back fixture [also provides an external clock reference].

Interrupts are supported by IP-BiSerial-VI-SIB. A force interrupt for software development and test is provided plus an interrupt from various serial port functions. Status is provided separate from the interrupt to allow use in a polled environment as well.

Address Maps

Address Map Base

IPBISVI_SIB_BASE	0x00 //0 Base control register
IPBISVI_SIB_VECTOR	0x02 //1 Interrupt vector register
IPBISVI_SIB_BASE_STATUS	0x04 //2 status read
IPBISVI_SIB_INFO	0x06 //3 Spare port used by OS
IPBISVI_SIB_REV	0x08 //4 Revision, Major&Minor, read only
IPBISVI_SIB_GATECNT	0x1E //15 GateCount
IPBISVI_SIB_CH0	x20 ⇔ 0x36 //16-27 Address range channel 0
IPBISVI_SIB_CH1	x38 ⇔ 0x4E //28-39 Address range channel 1

FIGURE 4 IP-BISERIAL-VI-SIB BASE ADDRESS MAP

Address Map Channel

IPBISVI_SIB_CHAN	0x00 //0 Channel control register
IPBISVI_SIB_CHAN_STAT	0x02 //1 Chanel Status Register
IPBISVI_SIB_AlmostFull	0x04 //2 Compare value for Rx Almost Full
IPBISVI_SIB_AlmostEmpty	0x06 //3 Compare value for Tx Almost Empty
IPBISVI_SIB_FIFO	0x08 //4 Read Rx Write TX FIFO
IPBISVI_SIB_CheckCount	0x0A //5 Read Reference Count
IPBISVI_SIB_TxFifoCnt	0x0C //6 Read Tx FIFO Data Count
IPBISVI_SIB_RxFifoCnt	0x0E //7 Read Rx FIFO Data Count

FIGURE 5 IP-BISERIAL-VI-SIB CHANNEL ADDRESS MAP

Numbers following the // are the HW decode numbers based on the words – word 0, word 1 etc. There are a total of 64 available in the IP IO space.

Programming

Programming IP-BiSerial-VI-SIB requires only the ability to read and write data from the host. The base address refers to the first user address for the slot in which the IP is installed.

The registers are organized in a heirarchy. The base level has card level control and information. The channels repeat with the same relative offsets to the start of each address range shown.

For example IPBISVI_SIB_CHAN_STAT in channel 1 = Base Address + Channel 1 starting address + IPBISVI_SIB_CHAN_STAT offset = Base + x38 + x2 = x3A plus the base address from the system.

Depending on the software environment it may be necessary to set-up the system software with IP-BiSerial-VI-SIB "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware. Other OS may be more “plug and play”. The Dynamic Engineering Driver operates in a “plug and play” mode using parent ⇔ child architecture.

If the special functions are used, access to the IO space is utilized. The bit maps for the IO space registers follows in the next section.

Interrupts are available to alert the local host when an event has happened.

The Dynamic Engineering IP-BiSerial-VI-SIB drivers for Windows WFM (7), Linux, and VxWorks manage the interaction and can set-up the transfer for you. Please refer to the driver manuals for more information.

Register Definitions Base

IPBISVI_SIB_BASE

0x0000 // 0 base control register offset

BASE Control Register

DATA BIT	DESCRIPTION
15	PLL_SDAT
14	spare
13	PLL_SCLK
12	PLL_EN
11	SdClkEn
10-5	spare
4	MasterChanEn
3	spare
2	IntForce
1	IntMasterEn
0	CLK8_32

FIGURE 6 IP-BISERIAL-VI-SIB BASE CONTROL REGISTER BIT MAP

CLK8_32: Can be used to tell the IP what the IP Clock rate is. Currently unused in this design.

IntMasterEn: when set allows programmed interrupt sources to assert Int0. Required for all interrupt types.

Intforce: when set causes an interrupt to be generated to the system. Useful for debugging and software test.

MasterChanEn: is used in conjunction with the channel controls to create grouped channels for purposes of start-up. For example to start the channels together, clear this bit and use the channel controls to use the master enable, plus enable within the channel. Once set-up, use this master enable to release all of the programmed channels.

SdClkEn: when set enables the upper IO to provide a reference 25 KHz clock for loop-back testing in SDC/SDT mode. Normally disabled.

PLL IF programming.
The PLL reference frequency is 50 MHz. The PLL is a Cypress 22393. The PLL is programmed with the output file generated by the Cypress PLL programming tool. [CY3672 R3.01 Programming Kit or CyberClocks R3.20.00 or later.]

The .JED file is used by the Dynamic Driver to program the PLL. Programming the PLL is fairly involved and beyond the scope of this manual. For clients writing their own drivers it is suggested to get the Engineering Kit for this board including software, and to use the translation and programming files ported to your environment. This procedure will save you a lot of time. The output file from the Cypress tool can be passed directly to the Dynamic Driver [Linux or Windows] and used to program the PLL.

pll_en : Software output enable control for PLL
pll_sclk: Output to pll command clock
pll_s2 : grounded on the card.
pll_sdat : When PLL_EN is set the output follows the register bit otherwise held in tristate. When read the state of the IO pin is returned.

Please note: the PLL is not currently used in this design.

IPBISVI_SIB_VECTOR
0x0002 // 1 IP vector port

Vector Port

DATA BIT	DESCRIPTION
15-8	Spare
7-0	vector

FIGURE 7 IP-BISERIAL-VI-SIB VECTOR BIT MAP

If the system uses a vectored interrupt approach then the vector port should be initialized to the vector value assigned to this device. IP-BiSerial-VI-SIB can be used as vectored or auto-vectored. In auto-vectored situations this port is unused. The Status port can be used to determine the source of any pending interrupts from IP-BiSerial-VI-SIB.

Default is 0xFF for data.

IPBISVI_SIB_BASE_STATUS

0x0004 // 2 base Status register

Status Register

DATA BIT	DESCRIPTION
15	IntReq
14-12	set to 0 currently
11	SdcSdtCompleteLat
10	IdleStateSdcSdtTst
9-2	set to 0 currently
1	IntReq1
0	IntReq0

FIGURE 8 IP-BISERIAL-VI-SIB INTERRUPT STATUS BIT MAP

IntReq1-0: when set indicates the corresponding channel has an interrupt request pending. Signal level before the Master Interrupt Enable.

IntReq When any of the IntReq0-1 are set or ForceInt is set and the Master Interrupt Enable is set this bit will be set.

IdleStateSdcSdtTst When set the SDC / SDT gate simulator is in the IDLE state. When not set, the simulator is active.

SdcSdtCompleteLat When set the SDC / SDT gate simulator has completed the programmed transfer. Captured and held. Write back with '1' in this bit position to clear.

IPBISVI_SIB_INFO

0x0006 // 3

Location Register

DATA BIT	DESCRIPTION
15-11	spare
10-3	Carrier Switch
2-0	Carrier Slot

FIGURE 9 IP-BISERIAL-VI-SIB INFO BIT MAP

The location register can be updated by the carrier driver during initialization. The IP-BiSerial-VI-SIB Driver can access this information later to determine the carrier and location on the carrier that this node is installed into. Once the IP-BiSerial-VI-SIB Driver is started the user software can use this as a general purpose register. The IP Driver stores a local copy in RAM to allow the user software to determine which node it is talking to when multiple nodes are present in a PCI/PCIe based system with dynamic addressing. Please note that this function is supported on all Dynamic Engineering carriers and may not be supported on other products.

In a Windows system the user software will query for the installed devices and the devices will be returned in order. The issue is that the order can change and there is no way to directly tell with software which card you are controlling at the moment. The user software can retrieve the devices present and then match them up to the physical hardware based on the carrier switch setting and slot on the carrier.

In some systems knowing which board is controlling which machine can be important. Please see the software manual and userap reference software for examples of working with multiple cards. The userap software prints out the device number and associated slot and switch settings. Your software can use the information without printing out for proper access control.

This is only important if you have multiple cards visible to the same CPU.

Register is optional for use.

IPBISVI_SIB_REV

0x0008 // 4

Node Address and Options Register

DATA BIT	DESCRIPTION
15-8	RevisionMajor
7-0	RevisionMinor

FIGURE 10 IP-BISERIAL-VI-SIB REVISION BIT MAP

RevisionMajor:
This field is reported via the IDPROM as well [revision]. It is rolled when major changes occur.

RevisionMinor:
This field is only read from this location. It is rolled when minor changes occur – usually during development to allow SW tracking of HW revisions without using the Major Revision field.

IPBISVI_SIB_ GATECNT

0x001E // 15

Node Address and Options Register

DATA BIT	DESCRIPTION
15-0	GateCount

FIGURE 11 IP-BISERIAL-VI-SIB GATE COUNT BIT MAP

GateCount, when written will cause the SDC SDT simulator to start operation. The stored count will program the length of the Gate signal generated. The external test fixture will connect the 4 GATE simulator outputs to the 4 Gate inputs plus the external clock references. The count is the number of words to send – a x1 will cause 16 bits to transfer. When the transfer is complete the event is flagged with the SdcSdtCompleteLat, readable in the Base Status Register.

If the count is larger than the FIFO size, additional data will need to be written to the transmitter and read from the receiver to avoid under/over flow conditions. See FIFO count section for FIFO size definition.

Register Definitions Channel

IPBISVI_SIB_CHAN

0x20, 38 // 0

CHANNEL CONTROL REGISTER

DATA BIT	DESCRIPTION
15	Enable
14	UseBaseEn
13	spare
12	CTSsense
11	CTSdisable
10	ClrCnt
9	IntForce
8	IntMasterEn
7	SwReset
6-2	Spare
1-0	ModeSel

FIGURE 12 IP-BISERIAL-VI-SIB CHAN BIT MAP

ModeSel:
Set to 00 for SDT/SDC, and 10 for USOP/USIP. Undefined combinations are unused and should not be selected.

SwReset:
Set to '1' to cause a local reset to the SIB state machine. Control registers unaffected. Return to '0' to resume normal operation. No minimum reset width required.

IntMasterEn: when set allows programmed interrupt sources to assert an interrupt request to the Base level of the design. Required for all interrupt types.

Intforce: when set causes an interrupt to be generated to the system. Useful for

debugging and software test. Requires IntMasterEn to be set both in the channel and the base.

ClrCnt
Set to ‘1’ to cause the Reference Counter to reset. Return to ‘0’ to resume counter operation. Use to synchronize counter for external clock check test. See CheckCount register for more detail.

CTSdisable:
Set to ‘1’ to force the CTS control into not enabled for transfer – the transmitter will detect and stop sending data or not start in the first place.

CTSsense:
Determine the active and disabled definition of the CTS control signal. ‘0’ correlates to CTS = ‘1’ when Cleared to Send, and ‘0’ for Not Cleared to Send. ‘1’ inverts with CTS = ‘0’ for Cleared to Send and ‘1’ for Not Cleared to send. Note: this definition controls output sense when CTSdisable is active.

For more about CTS see the Almost Full register definition.

UseBaseEn:
Set to ‘1’ to require both the channel Enable and the Base Enable to be set to allow this channel to operate. When set multiple channels can be started together. When ‘0’ the Base Control Register Enable is ignored and the channel starts with the channel Enable exclusively.

Enable:
Set to ‘1’ to start operation. When changing modes read the Status register and make sure in Idle before setting this bit.

IPBISVI_SIB_CHAN_STAT

0x22, 3A // 1

CHANNEL STATUS Register

DATA BIT	DESCRIPTION
15-12	'0'
11	RxFifoOverFlowLat
10	RxFifoFull
9	RxFifoAlmostFull
8	RxFifoMt
7	CTSOP
6	TxFifoFull
5	TxFifoAlmostMt
4	TxFifoMt
3	RxIdleState
2	TxIdleState
1	RxIntReqSmLat
0	TxIntReqSmLat

FIGURE 13 IP-BISERIAL-VI-SIB CHANNEL STATUS BIT MAP

(Tx,Rx)IntReqSmLat:
When '1' the (Tx/Rx) State Machine has reached completion. When Gate is de-asserted the SM's consider it an end of message event and set the bit(s). With the SDT/SDC mode, Gate is an external signal for both. For USOP/USIP the Gate signal is driven by the USOP and received by USIP. The Transmitter may be held off by CTS when requires the Gate to be deasserted. The receiver will create an interrupt request, reading the data will reduce the count and automatically enable CTS for more transfers. Depending on the speed of the CPU and the length of the message several interrupts may occur to manage 1 message. For messages smaller than the defined Almost Full length [assuming an empty FIFO to start] only 1 interrupt per message is expected. The transmitter will also create interrupts under these conditions. Clear by writing back with the same bit(s) set.

(Tx,Rx)IdleState:
When '1' the State Machine(s) is/are in the Idle State and ready to be enabled. Check this bit when changing modes.

(Tx,Rx)FifoMt is set '1' when there is no data in the corresponding FIFO.

TxFifoAlmostMt is set when the Tx FIFO meets the programmed Almost Empty criteria. Refer to the Tx Almost Empty register for more.

RxFifoAlmostFull is set when the Rx FIFO meets the programmed Almost Full criteria. Refer to the Rx Almost Full register for more.

(Tx,Rx)FifoFull is set '1' when there is no additional room for data in the corresponding FIFO.

CTSOP: This bit reflects the line state of the Transmit Side CTS signal. What the transmitter is using to determine if allowed to transmit or not in USOP. Synchronized by IP clock and otherwise not processed/filtered.

RxFifoOverFlowLat: If the Rx FIFO is written to when full an overflow event occurs. This bit is set when this happens. Held until cleared. Write back with '1' in this position to clear.

IPBISVI_SIB_AlmostFull

0x24, 3C // 2

CHANNEL Almost Full Register

DATA BIT	DESCRIPTION
15-0	Almost Full Value

FIGURE 14 IP-BISERIAL-VI-SIB ALMOST FULL

The channel Almost Full value is set to control when CTS is asserted in relationship to data in the receive FIFO. Status based on this condition is also available in the Status Register. The Receive FIFO is 511x16. Setting values larger than the FIFO size should not be implemented. The value is in words. X10 less than the Full condition is recommended to allow the transmitter to detect and stop transmitting before hitting the overflow condition.

USOP is held off by CTS for start-up. If de-asserted during a transfer USOP will detect the event and stop sending – “gracefully” remove Gate and stop advancing the data, then wait for CTS to be in the operational state. Depending on where the signal is detected in relation to the currently transmitted word, USOP may stop on the current word or the next word.

IPBISVI_SIB_AlmostEmpty

0x26, 3E // 3

CHANNEL Almost Empty Register

DATA BIT	DESCRIPTION
15-0	Almost Empty Value

FIGURE 15 IP-BISERIAL-VI-SIB ALMOST EMPTY

The channel Almost Empty value is set to control when the Channel Status TxFifoAlmostEmpty is set. The Transmit FIFO is 511x16. Setting values larger than the FIFO size should not be implemented. The value is in words. Set to a value large enough to allow SW to add more data to the transmitter without going empty for larger than FIFO size messages. The amount will depend on the OS. For messages that can be completely contained within the FIFO this bit can usually be ignored.

IPBISVI_SIB_FIFO

0x28, 40 // 4

CHANNEL FIFO(s)

DATA BIT	DESCRIPTION
15-0	Data

FIGURE 16 IP-BISERIAL-VI-SIB FIFO

Writing to this address will load data into the TX FIFO. Reading from this address will fetch data from the RX FIFO. Reading the Count registers will allow a tight loop to load or read without risk of overflowing or underflowing.

IPBISVI_SIB_CheckCount

0x2A, 42 // 5

CHANNEL Check Count Register

DATA BIT	DESCRIPTION
15-8	IP Count
7-0	Reference Count

FIGURE 17 IP-BISERIAL-VI-SIB CHECK COUNT BIT MAP

SIB uses a locally derived 1 MHz clock reference to transmit in USOP mode. The counter can check if this clock is present and approximately the correct frequency.

Recommended procedure: Reset the counter [counts 0=> FF] to 0x00. Enable the counter and poll the IP clock count. When mid range ~ 128 capture the result and compare the IP count with the Reference Count. With an 8 MHz IP clock and a 1 MHz reference the ratio should be near 8. The ratio will only be exact 1 out of 8 clocks since the Ref side only increments at the lower rate ⇔ look for a reasonable range rather than an absolute.

For a recurring non-interferring Bit test the count can be polled and if xffff reset and re-poll later. The counters do not roll over – park at xff. Clearing and releasing will result in the max count within 256 uS for the Ref Clock at 1 MHz case.

IPBISVI_SIB_TxFifoCnt

0x2C, 44 // 6

CHANNEL TX FIFO Count

DATA BIT	DESCRIPTION
15-0	Data

FIGURE 18 IP-BISERIAL-VI-SIB TX FIFO CNT

Reading from this address will return the count of the data words currently in the TX FIFO. Subtract from FIFO size to determine max write loop size for the TX FIFO port.

IPBISVI_SIB_RxFifoCnt

0x2E, 46 // 7

CHANNEL RX FIFO Count

DATA BIT	DESCRIPTION
15-0	Data

FIGURE 19 IP-BISERIAL-VI-SIB TX FIFO CNT

Reading from this address will return the count of the data words currently in the RX FIFO. Subtract from FIFO size to determine max read loop size for the RX FIFO port.

Interrupts

IP-BiSerial-VI-SIB interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with an IP-BiSerial-VI-SIB interrupt the software must read the status register(s) to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

The interrupt is mapped to INT0 on the IP connector, which is mapped to a system interrupt via the host [carrier] device. The source of the interrupt is obtained by reading the Interrupt Status registers. The status remains valid until that bit in the status register is cleared.

When an interrupt occurs, the Master channel interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the status and enable the channel interrupt again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the Interrupt Status register.

The base level has a master interrupt enable that affects all interrupt sources. This bit will also need to be enabled; in addition to the channel interrupt enables.

JTAG

IP-BiSerial-VI-SIB supports JTAG programming of the FLASH. J2 is a low profile connector that can accept standard .025” sq posts. Dynamic Engineering uses the flying lead option with the Impact USB programmer plus a standard header to interconnect. J2-1 = 3.3V, J2-2 = GND, J2-3 = TCK, J2-4 = TDO, J2-5 = TDI, J2-6 = TMS.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external connections. We used IP-Debug-IO interconnected as shown below.

There are 2 channels. Each channel has a transmitter and a receiver. With two modes per channel. 16 of the IO are used for the function. The remaining 8 are used for loop-back purposes.

SDC, SDT mode : gate and clock are inputs for both SDC and SDT. DataOut is tied to DataIn. The spare IO supply the Gate and CLK signals.

From signal – pins(P,N)	To signal- pins(P,N)
DataOP0-7,8	DataIP0-3,4
DataOP1-15,16	DataIP1-11,12
ExtClk0-21,22	ClkIP0-1,2
Extclk1-46,47	ClkOP0-5,6
ExtClk2-23,24	ClkIP1-9,10
ExtClk3-48,49	ClkOP1-13,14
GateOut0-17,18	GateIP0-26,27
GateOut1-42,43	GateOP0-30,31
GateOut2-19,20	GateIP1-34,35
GateOut3-44,45	GateOP1-38,39

USOP,USIP mode : cross connect outputs to inputs

From signal – pins(P,N)	To signal- pins(P,N)
ClkOP0-5,6	ClkIP0-1,2
DataOP0-7,8	DataIP0-3,4
GateOP0-30,31	GateIP0-26,27
CtsOP0-32,33	CtsIP0-28,29
ClkOP1-13,14	ClkIP1-9,10
DataOP1-15,16	DataIP1-11,12
GateOP1-38,39	GateIP1-34,35
CtsOP1-40,41	CtsIP1-36,37

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly. The revision is also readable from the base revision register where both the major [reported in the PROM] and minor fields are available.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-BiSerial-VI-SIB is shown in the figure below. For more information on IP ID PROM's refer to the IP Module Logic Interface Specification.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($0D) IP-BiSerial-VI
0D	Revision	($01)
0F	reserved	($31) Customer Number
11	Driver ID, low byte	($02) Design Number - SIB
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($BF)

FIGURE 20 IP-BISERIAL-VI-SIB ID PROM

IP-BiSerial-VI-SIB Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-BiSerial-VI-SIB. Pins marked n/c below are defined by the specification, but not used on the IP-BiSerial-VI-SIB. Also see the User Manual for your carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSEL*	4	29
D1	n/c	5	30
D2	MEMSEL*	6	31
D3	n/c	7	32
D4	INTSEL*	8	33
D5	n/c	9	34
D6	IOSEL*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTREG0*	17	42
D14	A4	18	43
D15	n/c	19	44
BS0*	A5	20	45
BS1*	n/c	21	46
n/c	A6	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 21 IP-BISERIAL-VI-SIB LOGIC INTERFACE

IP-BiSerial-VI-SIB IO Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-BiSerial-VI-SIB. Also see the User Manual for your carrier board for more information. IO#(signal name). Schematic shows IO#. Pairs are defined to be compatible with IP Standard Differential wiring – used on PCIe3IP, PCIe5IP etc.

IO0P(ClkIP0P)	IO1P(GateIP0P)	1	26
IO0N(ClkIP0N)	IO1N(GateIP0N)	2	27
IO2P(DataIP0P)	IO3P(CtsIP0P)	3	28
IO2N(DataIP0N)	IO3N(CtsIP0N)	4	29
IO4P(ClkOP0P)	IO5P(GateOP0P)	5	30
IO4N(ClkOP0N)	IO5N(GateOP0N)	6	31
IO6P(DataOP0P)	IO7P(CtsOP0P)	7	32
IO6N(DataOP0N)	IO7N(CtsOP0N)	8	33
IO8P(ClkIP1P)	IO9P(GateIP1P)	9	34
IO8N(ClkIP1N)	IO9N(GateIP1N)	10	35
IO10P(DataIP1P)	IO11P(CtsIP1P)	11	36
IO10N(DataIP1N)	IO11N(CtsIP1N)	12	37
IO12P(ClkOP1P)	IO13P(GateOP1P)	13	38
IO12N(ClkOP1N)	IO13N(GateOP1N)	14	39
IO14P(DataOP1P)	IO15P(CtsOP1P)	15	40
IO14N(DataOP1N)	IO15N(CtsOP1N)	16	41
IO16P(GateOut0P)	IO17P(GateOut1P)	17	42
IO16N(GateOut0N)	IO17N(GateOut1N)	18	43
IO18P(GateOut2P)	IO19P(GateOut3P)	19	44
IO18N(GateOut2N)	IO19N(GateOut3N)	20	45
IO20P(ExtClk0P)	IO21P(ExtClk1P)	21	46
IO20N(ExtClk0N)	IO21N(ExtClk1N)	22	47
IO22P(ExtClk2P)	IO23P(ExtClk3P)	23	48
IO22N(ExtClk2N)	IO23N(ExtClk3N)	24	49
IO_GND	IO_GND	25	50

NOTE: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

FIGURE 22 IP-BISERIAL-VI-SIB IO CONNECTOR PINOUT

IO_GND = AC / DC / Open based on J1 header shunt setting.

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions were chosen with noise immunity and cable compatibility in mind. The pairs should be connected with twisted pair wiring compatible with a 100 ohm system for best results.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the 485/LVDS devices rated voltages.

If induced noise is causing errors, please check the cabling and make sure the shields are properly tied to ground on one side. It may be necessary to go to higher grade cable. Please note that the shield ground on the card is connected to a header to allow user programming to a DC ground, AC [.1uF cap to ground] or open.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-BiSerial-VI-SIB is constructed out of 0.062 inch thick high temp ROHS compliant FR4 material.

Options are available for ROHS and standard processing of the SRAM based versions with either connector type. The FRAM option is only available with ROHS processing.

Through hole and surface mounting of components are used.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of .89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if .89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-BiSerial-VI-SIB design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Host Interface:	IP Module 8 and 32 MHz capable
IO Interface:	2x 8 differential pairs [Gate, Clk, Data, CTS (Rx/Tx)] 2-511x16 FIFO per channel
Tx Data rates generated:	Internal clock rate is 1 MHz, External clocks are independent.
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers [except vector] to 0.
Access Modes:	IO, Memory, ID, INT spaces (see memory map)
Wait States:	minimized based on programmed clock rate
Interrupt:	Programmable per channel/mode
Onboard Options:	Most Options are Software Programmable. Shunt for IO ground reference: open, DC, AC
Interface Options:	24 differential pairs plus reference on P2.
Dimensions:	Type II
Construction:	High temp ROHS compatible FR4 Multi-Layer Printed Circuit, Through Hole and SMT.
Temperature Coefficient:	.89 W/^{o}C for uniform heat across IP
Power:	Typical **180** mA @ 5V typical.
Temperature Range	–40C⇔85C or better, rated components. Conformal Coating option for condensing environments

Order Information

IP-BiSerial-VI-SIB	IP Module with SDT/SDC and USOP/USIP capability. 2 ports each with Gate, Clk, Data, CTS input and output. Internal clock reference is 1 MHz – 1 uS pulse granularity.
-CC	Conformal Coating option
-ROHS	Change to ROHS processing. Without this option, standard leaded solder will be used.
-LVDS	RS-485 is standard for this design. To receive with LVDS IO add this option.
Eng Kit–IP-BiSerial-VI-SIB	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender IP-BiSerial-VI-SIB Driver and reference software Technical Documentation, 1. IP-BiSerial-VI-SIB Schematic Data sheet reprints are available from the manufacturer's web site reference software.

Note: The Engineering Kit is strongly recommended for first time purchases.

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not guaranteed to be current or complete manufacturing data, nor is it part of the product specification.