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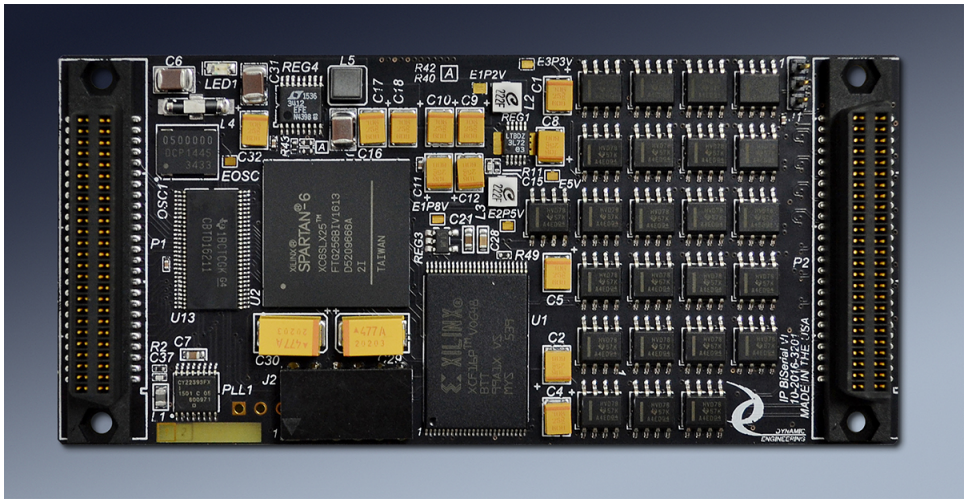
Est. 1988

User Manual

IP-BiSerial-VI-CTRB

Counter Timer / One Shot Interface

RS485
IndustryPack® Module



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FLASH revision: Std 0104 Fab: 10-2016-3201

IP-BiSerial-VI-CTRB
Counter Timer / One Shot
IndustryPack® Module

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

IP-BiSerial-VI-CTRB is implemented using IP-BiSerial-VI outfit with 24 RS-485 transceivers. The FLASH loaded manifests the CTRB specification as decribed below.

IP-BiSerial-VI is part of the IndustryPack® "IP" Module family of I/O components by Dynamic Engineering. IP-BiSerial-VI provides an IP Module type II compliant mechanical package with a Spartan 6 FPGA, FLASH, PLL(4 reference clocks to FPGA), 24 differential IO [LVDS and/or RS485] each with separately programmable terminations and direction controls. The FLASH is easily reprogrammable with the Xilinx Impact SW and USB adapter – there is a header for this purpose.

The Differential IO are routed to the connector with controlled impedance, matched length [FPGA to IO pin pairs], and pin definitions consistent with the Dynamic Engineering standard for differential IO on IP Modules [1,2 … 23,24 (25,50 grounds), 26,27…48,49]. This definition is implemented on Dynamic Engineering Carrier designs supporting differential pairs [PCIe3IP, PCIe5IP, PCI3IP, PCI5IP, VPX2IP] to name a few.

CTRB is designed with a two level hierarchy – Base and Channel. The Base level has the IP Bus interface and decoding, master interrupt control, PLL programming [unused], clock generation, and Channel instantiation. Each of the 8 channels has the same capabilities. Counter and One Shot support with several programmable options discussed in the following paragraphs.

In the Counter Modes the options are for internal and external clock input, length of time until the timer expires, continuous or single count down, interrupt or polled operation.

In the One Shot Modes the options include internal or external clock reference, internal or external trigger, rising or falling edge [with external trigger], length of output pulse, interrupt or polled operation.

The internal reference clock is 1 MHz and is derived from the 50 MHz oscillator. The oscillator frequency is divided down to 2 MHz and distributed to the channels. Within each channel the 2 MHz is divided to 1 MHz and muxed with the external clock. IP-BiSerial-VI features 8 clockout/clock in pairs [IO connections between closely located pins where an IO is tied to a clock input pin]. This allows the muxed signal to be brought back into the FPGA and treated as a clock [Channel Reference Clock] With a lower number of channels the internal clock muxes could be used. With 8 channels resource limitations makes this approach problematic. This feature was borrowed from PMC-BiSeral-VI.

External signals are synchronized to the Channel Reference Clock before being checked by the CTRB State Machine.

The CTRB SM has several states to accomplish the Counter and One Shot modes.

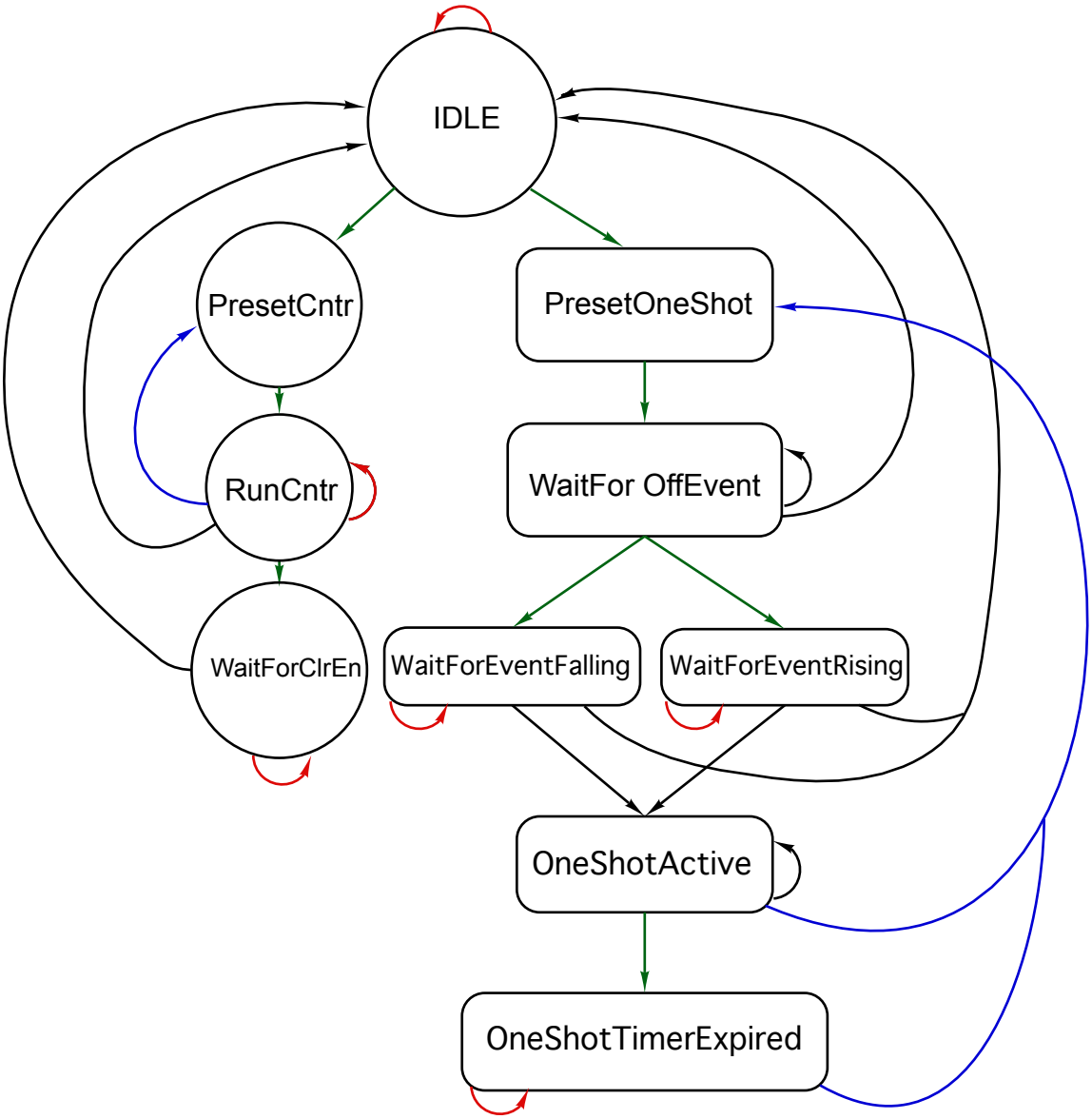

FIGURE 1 IP-BISERIAL-VI-CTRB STATE FLOW DIAGRAM

Blue represents re-arming paths. Red for delay paths. Green for Advance paths. Black for return to IDLE. Return to Idle can happen if the Enable is disabled. It is recommended to return to the IDLE state when changing modes of operation.

When Enabled the channel state-machines will advance to the Preset Counter or Preset One Shot states based on the programmed mode. Each channel is independent.

For the Counter modes (Auto, Normal) the 32 bit down counter is preloaded and the count started. In the Run Counter state the count is compared and when it is almost completed the state is advanced to restart in the Preset Counter state [Auto] or to the Wait for Clear Enable [Normal] state. When leaving The Run Counter state the output pulse is programmed as well as the clear for the enable if in the Normal mode. In Auto mode the clear is not asserted and looping behavior results. Coincident with the Pulse generation is the interrupt request assertion.

Preset One Shot also loads the 32 bit counter in anticipation of a trigger event. Once loaded the state machine advances to the Wait For Off Event state. The state-machine remains here until the programmed event is in the opposite state allowing for a potential edge to be detected. For example if the falling edge and external trigger options are programmed and the line is low the state machine will remain in the Wait state since a falling edge is not possible.

Once the trigger is in the correct state for the programmed option, the state-machine will advance to wait for the Rising or Falling edge. The Software Trigger option is always the rising edge. The state-machine waits until the programmed edge is detected. With the assertion of the programmed condition, the state-machine advances to the One Shot Active state where the external pulse is asserted and the counter is activated.

In this mode the counter is the time of the pulse rather than the time between pulses. Once the time is almost completed the termination sequence begins to provide the proper pulse width. The state-machine will in the case of the Software Trigger – clear the trigger and wait for it to be cleared. With External triggers the state-machine advances directly to the Preset state. An interrupt can be generated coincident with the end of the pulse.

The interrupt request is maskable at the channel to allow polled operation. In addition status for several of the state-machine states is available to “know” when in the Idle, Armed or Active One Shot states. Armed means waiting for trigger. If not Idle or Armed or Active then the SM is likely waiting for the external line to be in the correct state as noted above.

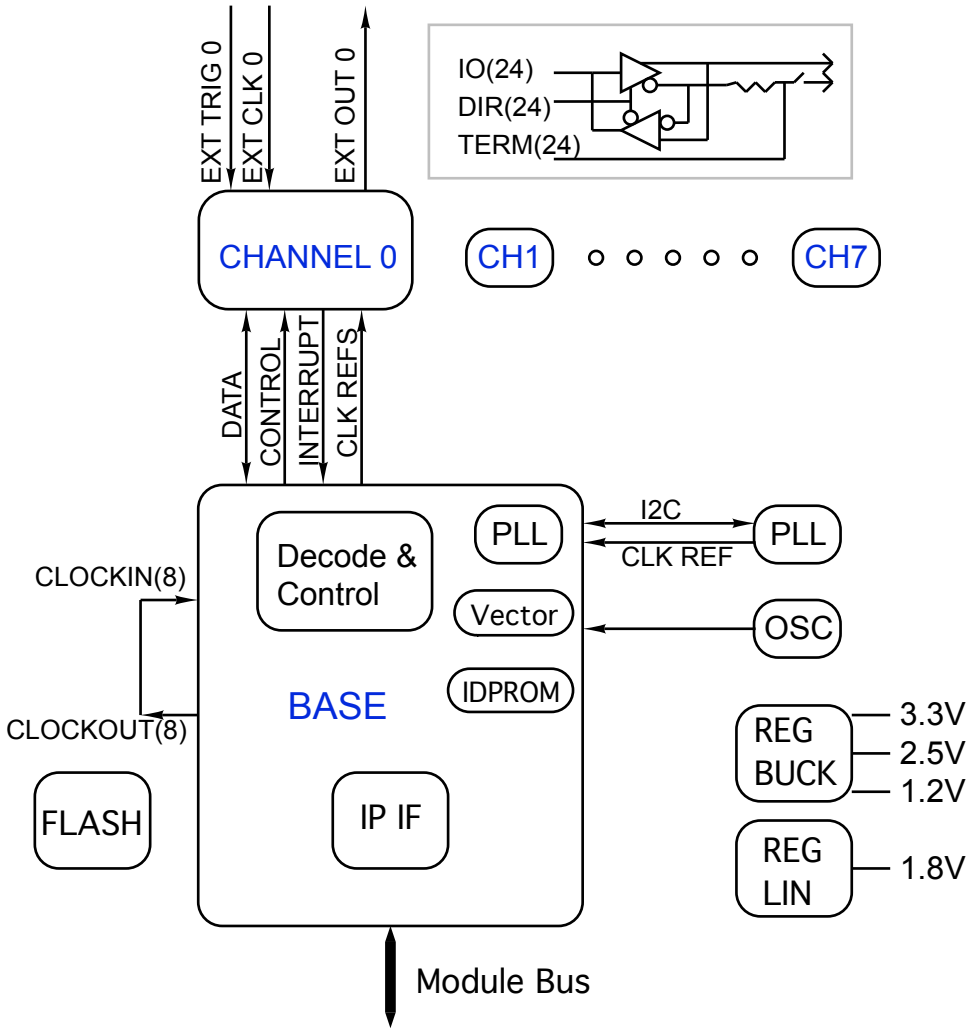

FIGURE 2 IP-BISERIAL-VI-CTRB BLOCK DIAGRAM

IP-BiSerial-VI incorporates 24 differential pairs, each of which can be LVDS or RS485. For CTRB, RS485 is implemented with each of the 8 channels using 3 of the IO. Each channel has two inputs – External Clock and External Trigger, plus one output – External Out. Within each channel is the state-machine shown in Figure 1 and the supporting logic for independent operation.

The Spartan VI requires three voltages, derived via Buck regulators from the 5V IP

standard voltage [3.3V, 2.5V, and 1.2V]. In addition the FLASH requires a small amount of 1.8V and a linear regulator is provided for this purpose. The 3.3V rail is also used for the LVDS and RS-485 devices allowing mix and match assembly.

The PLL is provided but not used in the CTRB Design. The installed oscillator is a 50 MHz model with 10 ppm. Additional board level clocking options include the ClockOut to ClockIn network. Each of the 8 ClockOut signals is tied back to a clock input on the FPGA allowing flexibility. This clock bus is used within CTRB to allow each channel to use either the external reference or internal reference with the same clock input pin.

The FLASH is used to store the module firmware – in this case the CTRB function.

The Base level of the design provides the IndustryPack interface, general decoding, card level status, IDPROM and Vector register plus board level features ⇔ PLL, interrupt masking, master channel enable.

Each Channel is the same in the case of CTRB. The decoded data bus is routed to each channel along with decoded read and write controls to allow SW control over channel assets. Each channel has a control register, status register, counter definition register [32 bit] and reference clock counter read-back.

Please refer the address/bit maps for details of the various registers and operation.

The External Trigger when used in One Shot mode has an inline filter built in. The filter operates from the IP clock allowing the user to set to ~250 nS or ~62.5 nS based on 8 or 32 MHz operation.

IP-BiSerial-VI-CTRB conforms to the IndustryPack® standard. This guarantees compatibility with compliant carrier boards. Because the IP-BiSerial-VI-CTRB may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCIe3IP – PCI carrier for IP Modules can be used for development in a conventional PC. Later the hardware and software can be ported to the target. http://www.dyneng.com/PCIe3IP.html

With the Dynamic Engineering Windows driver collection for IP and carrier modules a Parent – Child architecture is employed. The IP portion of the driver is directly portable between the various Dynamic Engineering IP carriers [PCIe3IP, PCI3IP, PCIe5IP, PCI5IP, PC104pIP, PC104p4IP, cPCI2IP, cPCI4IP etc]. The parent portion of the driver contains the carrier specific design information. This means that software developed for the IP-BiSerial-VI-CTRB on one platform can be directly ported to another. PCI to cPCI for example.

Designers can make use of the Dynamic Engineering carrier driver for non-Dynamic Engineering IP modules using the Generic IP capability built into the parent portion of the driver. IP modules that the carrier driver does not recognize are installed as "generic" and accessed with a address, data interface model. Software developed for the Generic mode can also be ported between modules.

IP-BiSerial-VI-CTRB is tested with a combination of internal and external tests. The registers can be tested with R/W tests, the channels can be tested with the external loop-back fixture [also provides an external clock reference].

Interrupts are supported by IP-BiSerial-VI-CTRB. A force interrupt for software development and test is provided plus an interrupt from end of count [counter timer mode] or end of pulse [one shot]. Status is provided separate from the interrupt to allow use in a polled environment as well.

Address Maps

Address Map Base

IPBISVI_CTRB_BASE	0x00 //0 Base control register
IPBISVI_CTRB_VECTOR	0x02 //1 Interrupt vector register
IPBISVI_CTRB_BASE_STATUS	0x04 //2 status read
IPBISVI_CTRB_INFO	0x06 //3 Spare port used by OS
IPBISVI_CTRB_REV	0x08 //4 Revision, Major&Minor, read only
IPBISVI_CTRB_CH0	x20 ⇔ 0x2A //16-21 Address range channel 0
IPBISVI_CTRB_CH1	x2C ⇔ 0x36 //22-27 Address range channel 1
IPBISVI_CTRB_CH2	x38 ⇔ 0x42 //28-33 Address range channel 2
IPBISVI_CTRB_CH3	x44 ⇔ 0x4E //34-39 Address range channel 3
IPBISVI_CTRB_CH4	x50 ⇔ 0x5A //40-45 Address range channel 4
IPBISVI_CTRB_CH5	x5C ⇔ 0x66 //46-51 Address range channel 5
IPBISVI_CTRB_CH6	x68 ⇔ 0x72 //52-57 Address range channel 6
IPBISVI_CTRB_CH7	x74 ⇔ 0x7E //58-63 Address range channel 7

FIGURE 3 IP-BISERIAL-VI-CTRB BASE ADDRESS MAP

Address Map Channel

IPBISVI_CTRB_CHAN	0x00 //0 Channel control register
IPBISVI_CTRB_CHAN_STAT	0x02 //1 Chanel Status Register
IPBISVI_CTRB_PreLoadLwr	0x04 //2 PreLoad register lower 16
IPBISVI_CTRB_PreLoadUpr	0x06 //3 PreLoad register upper 16
IPBISVI_CTRB_CheckCount	0x08 //4 Read Reference Count

FIGURE 4 IP-BISERIAL-VI-CTRB CHANNEL ADDRESS MAP

Numbers following the // are the HW decode numbers based on the words – word 0, word 1 etc. There are a total of 64 available in the IP IO space.

Programming

Programming IP-BiSerial-VI-CTRB requires only the ability to read and write data from the host. The base address refers to the first user address for the slot in which the IP is installed.

The registers are organized in a heirarchy. The base level has card level control and information. The channels repeat with the same relative offsets to the start of each address range shown.

For example IPBISVI_CTRB_CHAN_STAT in channel 1 = Base Address + Channel 1 starting address + IPBISVI_CTRB_CHAN_STAT offset = Base + x2C + x2 = x2E plus the base address from the system.

Depending on the software environment it may be necessary to set-up the system software with IP-BiSerial-VI-CTRB "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware. Other OS may be more “plug and play”. The Dynamic Engineering Driver operates in a “plug and play” mode using parent ⇔ child architecture..

If the special functions are used, access to the IO space is utilized. The bit maps for the IO space registers follows in the next section.

Interrupts are available to alert the local host when an event has happened.

The Dynamic Engineering IP-BiSerial-VI-CTRB drivers for Windows WFM (7+), Linux, and VxWorks manage the interaction and can set-up the transfer for you. Please refer to the driver manuals for more information.

Register Definitions Base

IPBISVI_CTRB_BASE

IPBISVI_CTRB_BASE 0x0000 // 0 base control register offset

BASE Control Register

DATA BIT	DESCRIPTION
15	PLL_SDAT
14	spare
13	PLL_SCLK
12	PLL_EN
11-5	spare
4	MasterChanEn
3	spare
2	IntForce
1	IntMasterEn
0	CLK8_32

FIGURE 5 IP-BISERIAL-VI-CTRB BASE CONTROL REGISTER BIT MAP

CLK8_32: Can be used to tell the IP what the IP Clock rate is. Currently unused in this design.

IntMasterEn: when set causes allows programmed interrupt sources to assert Int0. Required for all interrupt types.

Intforce: when set causes an interrupt to be generated to the system. Useful for debugging and software test.

MasterChanEn: is used in conjunction with the channel controls to create grouped channels for purposes of start-up. For example if in auto mode and want the various timers to start together, clear this bit and use the channel controls to use the master enable, plus enable within the channel. Once set-up, use this master enable to release all of the programmed channels. Not all channels have to be affected – the channels can be left in independent mode where this bit is ignored.

PLL IF programming.
The PLL reference frequency is 50 MHz. The PLL is a Cypress 22393. The PLL is programmed with the output file generated by the Cypress PLL programming tool. [CY3672 R3.01 Programming Kit or CyberClocks R3.20.00 or later.]

The .JED file is used by the Dynamic Driver to program the PLL. Programming the PLL is fairly involved and beyond the scope of this manual. For clients writing their own drivers it is suggested to get the Engineering Kit for this board including software, and to use the translation and programming files ported to your environment. This procedure will save you a lot of time. The output file from the Cypress tool can be passed directly to the Dynamic Driver [Linux or Windows] and used to program the PLL.

pll_en : Software output enable control for PLL
pll_sclk: Output to pll command clock
pll_s2 : grounded on the card.
pll_sdat : When PLL_EN is set the output follows the register bit otherwise held in tristate. When read the state of the IO pin is returned.

Please note: the PLL is not currently used in this design.

IPBISVI_CTRB_VECTOR
IPBISVI_CTRB_Vector 0x0002 // 1 IP vector port

Vector Port

DATA BIT	DESCRIPTION
15-8	Spare
7-0	vector

FIGURE 6 IP-BISERIAL-VI-CTRB VECTOR BIT MAP

If the system uses a vectored interrupt approach then the vector port should be initialized to the vector value assigned to this device. IP-BiSerial-VI-CTRB can be used as vectored or auto-vectored. In auto-vectored situations this port is unused. The Status port can be used to determine the source of any pending interrupts from IP-BiSerial-VI-CTRB.

Default is 0xFF for data.

IPBISVI_CTRB_BASE_STATUS

IPBISVI_CTRB_BASE_STATUS 0x0004 // 2 base Status register

Status Register

DATA BIT	DESCRIPTION
15	IntReq
14-8	set to 0 currently
7	IntReq7
6	IntReq6
5	IntReq5
4	IntReq4
3	IntReq3
2	IntReq2
1	IntReq1
0	IntReq0

FIGURE 7 IP-BISERIAL-VI-CTRB INTERRUPT STATUS BIT MAP

IntReq7-0: when set indicates the corresponding channel has an interrupt request pending. Signal level before the Master Interrupt Enable.

IntReq When any of the IntReq0-7 are set or ForceInt is set and the Master Interrupt Enable is set this bit will be set.

IPBISVI_CTRB_INFO

IPBISVI_CTRB_INFO 0x0006 // 3

Location Register

DATA BIT	DESCRIPTION
15-11	spare
10-3	Carrier Switch
2-0	Carrier Slot

FIGURE 8 IP-BISERIAL-VI-CTRB INFO BIT MAP

The location register can be updated by the carrier driver during initialization. The IP-BiSerial-VI-CTRB Driver can access this information later to determine the carrier and location on the carrier that this node is installed into. Once the IP-BiSerial-VI-CTRB Driver is started the user software can use this as a general purpose register. The IP Driver stores a local copy in RAM to allow the user software to determine which node it is talking to when multiple nodes are present in a PCI/PCIe based system with dynamic addressing. Please note that this function is supported on all Dynamic Engineering carriers and may not be supported on other products.

In a Windows system the user software will query for the installed devices and the devices will be returned in order. The issue is that the order can change and there is no way to directly tell with software which card you are controlling at the moment. The user software can retrieve the devices present and then match them up to the physical hardware based on the carrier switch setting and slot on the carrier.

In some systems knowing which board is controlling which machine can be important. Please see the software manual and userap reference software for examples of working with multiple cards. The userap software prints out the device number and associated slot and switch settings. Your software can use the information without printing out for proper access control.

This is only important if you have multiple cards visible to the same CPU.

IPBISVI_CTRB_REV

IPBISVI_CTRB_REV 0x0008 // 4

Node Address and Options Register

DATA BIT	DESCRIPTION
15-8	RevisionMajor
7-0	RevisionMinor

FIGURE 9 IP-BISERIAL-VI-CTRB REVISION BIT MAP

RevisionMajor:
This field is reported via the IDPROM as well [revision]. It is rolled when major changes occur.

RevisionMinor:
This field is only read from this location. It is rolled when minor changes occur – usually during development to allow SW tracking of HW revisions without using the Major Revision field.

Register Definitions Channel

IPBISVI_CTRB_CHAN

IPBISVI_CTRB_CHAN 0x20, 2C, 38, 44, 50, 5C, 68, 74 // 0

CHANNEL CONTROL REGISTER

DATA BIT	DESCRIPTION
15	Enable
14	UseBaseEn
13	spare
12	spare
11	spare
10	ClrCnt
9	IntForce
8	IntMasterEn
7	SwReset
6	SwTrigger
5	ExtTriggerPol
4	ExtIntTrigger
3	ClkSel
2	spare
1-0	ModeSel

FIGURE 10 IP-BISERIAL-VI-CTRB CHAN BIT MAP

ModeSel:
Set to 00 for Counter Auto Mode, 01 for Counter Normal Mode, and 10 for One Shot. 11 is currently unused and should not be selected.

ClkSel:
Set to ‘1’ to use the external reference clock for channel operation, ‘0’ uses the internal 1 MHz clock. Affects all modes. The SM operats at the 1 MHz internal or external clock rate as selected. When changing from internal to external clocks or vice-versa it is recommended to change the clock, then cause a SW Reset to make sure any clock transition events are cleared.

ExtIntTrigger:
Set to ‘1’ for the external trigger input, Set to ‘0’ to use the SwTrigger. One Shot mode only.

ExtTriggerPol:
Set to ‘1’ for the rising edge, Set to ‘0’ for the falling edge. One Shot mode using the external trigger input only. [no affect otherwise]

SwTrigger:
Set to ‘1’ to cause the OneShot to trigger when in Internal mode. Do not use when in External mode. The PreLoad count value will determine the length of the output plus. Auto cleared when pulse is complete.

SwReset:
Set to ‘1’ to cause a local reset to the CTRB state machine. Control registers unaffected. Return to ‘0’ to resume normal operation. No minimum reset width required.

IntMasterEn: when set allows programmed interrupt sources to assert an interrupt request to the Base level of the design. Required for all interrupt types.

Intforce: when set causes an interrupt to be generated to the system. Useful for debugging and software test. Requires InMasterEn to be set both in the channel and the base.

ClrCnt
Set to ‘1’ to cause the Reference Counter to reset. Return to ‘0’ to resume counter operation. Use to synchronize counter for external clock check test. See CheckCount register for more detail.

UseBaseEn:
Set to ‘1’ to require both the channel Enable and the Base Enable to be set to allow this channel to operate. When set multiple channels can be started together. When ‘0’ the Base Control Register Enable is ignored and the channel starts with the Channel Enable exclusively.

Enable:
Set to ‘1’ to start operation. When changing modes read the Status register and make sure in Idle before setting this bit. Auto Cleared when in the Counter Normal Mode.

IPBISVI_CTRB_CHAN_STAT

IPBISVI_CTRB_CHAN_STAT 0x22, 2E, 3A, 46, 52, 5E, 6A, 76 // 1

CHANNEL STATUS Register

DATA BIT	DESCRIPTION
15	Current External Trigger In
14	OneShotWaiting
13-5	Spare
4	OneShotTimerLat
3	OneShotTimer
2	OneShotArmed
1	IdleState
0	IntReqSmLat

FIGURE 11 IP-BISERIAL-VI-CTRB CHANNEL STATUS BIT MAP

IntReqSmLat:
When '1' the State Machine has reached the completion of the programmed mode. The end of the programmed pulse length or programmed delay is used for this purpose. Clear by writing back with the same bit set.

IdleState:
When '1' the State Machine is in the Idle State and ready to be enabled. Check this bit when changing modes.

OneShotArmed:
When '1' the State Machine is in the states where the SW trigger or an external event can cause the OneShot to be activated. Please note: *this bit will not be set if the current input level is not where it needs to be in order to trigger*. For example if the current External Trigger Input is high and the rising edge is programmed for the trigger event, the SM will be in the state waiting for the low level before arming to check for a high state. Note: *Non-OneShot Modes do not use these states*. When using the SW Trigger, this bit should be checked before asserting the SW Trigger. It takes approximately 5 uS from clearing the SW Trigger to returning to the ARMed state in internal mode. Slightly shorter timing occurs in external mode.

OneShotTimer:
When '1' the State Machine is in the OneShot is active state. This bit is transitory and will only be asserted for the programmed pulse length. See the latched version.

OneShotTimer Lat:
When ‘1’ the State Machine at some point became active [pulse out driven for programmed time]. Useful for shorter pulses that might be missed via SW polling. Clear by writing back with the same bit set. When this bit is set it means the SM was active at some point, not necessarily active when it was read.

OneShotWaiting:
When ‘1’ the State Machine is in the state where the External Trigger In signal is not in the correct state to cause the one shot to be triggered. For example if the falling edge is programmed, the line will need to be ‘1’ to progress to the ARMed state. Note: Non-OneShot Modes does not use this state.

Current External Trigger In reflects the state of the external trigger in signal for the channel. Synchronized to the IP clock to allow reading, otherwise not filtered. If the HW appears stuck in OneShotWaiting this status bit can tell you what the SM is seeing and if the issue is with the line level or not.

Since the SM is operating at 1 MHz, as long as the Line goes to the correct level for at least 2 uS before the edge of interest, the edge will be seen.

IPBISVI_CTRB_PreLoad

IPBISVI_CTRB_PreLoadLwr, PreLoadUpr 0x24, 30, 3C, 48, 54, 60, 6C, 78 // 2,3

CHANNEL PreLoad Register(s)

DATA BIT	DESCRIPTION
31-0	PreLoad Value

FIGURE 12 IP-BISERIAL-VI-CTRB PRELOAD REGISTER BIT MAP

PreLoad:
Two 16 bit registers are LW aligned to allow 32 bit R/W operations to this locations. 16 bit accesses are also supported. D15-0 is the Lower half and 31-16 is the Upper Half.

The register is programmed with the count to use in both Counter and One Shot modes. In One Shot mode the count is used to determine the length of the output pulse. In Counter Modes [Normal and Auto] the count is used to determine the delay from pulse to pulse or enable to pulse.

The width / Time is N+1. Program 99 to get 100 uS for example.

Notes: When in Auto Mode the pulses will be the N+1 uS from same edge to same edge [pulse time is included]. When in Normal mode the delay to the pulse out is somewhat longer than programmed due to synchronizing SW Enable and the SM recognizing the bit has been set. This delay is minimized as much as possible. With Auto mode this is also the case, however since the pulses are now repeated the HW timing takes care of staying on time after the initial enable event.

In the One Shot mode the delay is minimized by waiting in the Armed state or one state prior depending on the line value. When the external trigger has been synchronized and recognized by the SM the pulse is output. This creates a 2-3 uS delay in most cases.

IPBISVI_CTRB_CheckCount

IPBISVI_CTRB_CheckCount 0x28, 34, 40, 4C, 58, 64, 70, 7C // 8

CHANNEL Check Count Register

DATA BIT	DESCRIPTION
15-8	IP Count
7-0	Reference Count

FIGURE 13 IP-BISERIAL-VI-CTRB CHECK COUNT BIT MAP

CTRB can be configured to use an external clock reference to operate the State-Machines, counters etc. Since the clock may not be present it is a good idea to check the Reference Clock is operating via the counter attached to this register.

Recommended procedure is to select the Internal or External Clock as needed. Reset the counter [counts 0=> FF] to 0x00. Enable the counter and poll the IP clock count. When mid range ~ 128 capture the result and compare the IP count with the Reference Count. With an 8 MHz IP clock and a 1 MHz reference the ratio should be near 8. The ratio will only be exact 1 out of 8 clocks since the Ref side only increments at the lower rate ⇔ look for a reasonable range rather than an absolute.

For a recurring non-interferring Bit test the count can be polled and if xffff reset and repoll later. The counters do not roll over – park at xff. Clearing and releasing will result in the max count within 256 uS for the Ref Clock at 1 MHz case.

Interrupts

IP-BiSerial-VI-CTRB interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with an IP-BiSerial-VI-CTRB interrupt the software must read the status register(s) to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

The interrupt is mapped to INT0 on the IP connector, which is mapped to a system interrupt via the host [carrier] device. The source of the interrupt is obtained by reading the Interrupt Status registers. The status remains valid until that bit in the status register is cleared.

When an interrupt occurs, the Master channel interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the status and enable the channel interrupt again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the Interrupt Status register.

The base level has a master interrupt enable that affects all interrupt sources. This bit will also need to be enabled; in addition to the channel interrupt enables.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external connections. We used IP-Debug-IO interconnected as shown below.

There are 8 channels. Each channel has an External Trigger(0), External Clk(1), and External Out(2) signal. There are 24 IO available leaving no spares.

The External Outs are daisy chained to the External Triggers. External Clocks are driven from an on-board oscillator/differential drivers(8) combination.

From	**To**
signal – pins(P,N)	signal- pins(P,N)
EO0-3,4	ET1-28,29
EO1-30,31	ET2-7,8
EO2-9,10	ET3-34,35
EO3-36,37	ET4-13,14
EO4-15,16	ET5-40,41
EO5-42,43	ET6-19,20
EO6-21,22	ET7-46,47
EO7-48,49	ET0-1,2

Clock SRC
EC0-26,27
EC1-5,6
EC2-32,33
EC3-11,12
EC4-38,39
EC5-17,18
EC6-44,45
EC7-23,24

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly. The revision is also readable from the base revision register where both the major [reported in the PROM] and minor fields are available.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-BiSerial-VI-CTRB is shown in the figure below. For more information on IP ID PROM's refer to the IP Module Logic Interface Specification.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($0D) IP-BiSerial-VI
0D	Revision	($01)
0F	reserved	($31) Customer Number
11	Driver ID, low byte	($01) Design Number-CTRB
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($63)

FIGURE 14 IP-BISERIAL-VI-CTRB ID PROM

IP-BiSerial-VI-CTRB Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-BiSerial-VI-CTRB. Pins marked n/c below are defined by the specification, but not used on the IP-BiSerial-VI-CTRB. Also see the User Manual for your carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSEL*	4	29
D1	n/c	5	30
D2	MEMSEL*	6	31
D3	n/c	7	32
D4	INTSEL*	8	33
D5	n/c	9	34
D6	IOSEL*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTREG0*	17	42
D14	A4	18	43
D15	n/c	19	44
BS0*	A5	20	45
BS1*	n/c	21	46
n/c	A6	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 15 IP-BISERIAL-VI-CTRB LOGIC INTERFACE

IP-BiSerial-VI-CTRB IO Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-BiSerial-VI-CTRB. Also see the User Manual for your carrier board for more information. IO#(signal name). Schematic shows IO#. Pairs are defined to be compatible with IP Standard Differential wiring – used on PCIe3IP, PCIe5IP etc.

IO0P(ExtTrig0P)	IO1P(ExtClk0P)	1	26
IO0N(ExtTrig0N)	IO1N(ExtClk0N)	2	27
IO2P(ExtOut0P)	IO3P(ExtTrig1P)	3	28
IO2N(ExtOut0N)	IO3N(ExtTrig1N)	4	29
IO4P(ExtClk1P)	IO5P(ExtOut1P)	5	30
IO4N(ExtClk1N)	IO5N(ExtOut1N)	6	31
IO6P(ExtTrig2P)	IO7P(ExtClk2P)	7	32
IO6N(ExtTrig2N)	IO7N(ExtClk2N)	8	33
IO8P(ExtOut2P)	IO9P(ExtTrig3P)	9	34
IO8N(ExtOut2N)	IO9N(ExtTrig3N)	10	35
IO10P(ExtClk3P)	IO11P(ExtOut3P)	11	36
IO10N(ExtClk3N)	IO11N(ExtOut3N)	12	37
IO12P(ExtTrig4P)	IO13P(ExtClk4P)	13	38
IO12N(ExtTrig4N)	IO13N(ExtClk4N)	14	39
IO14P(ExtOut4P)	IO15P(ExtTrig5P)	15	40
IO14N(ExtOut4N)	IO15N(ExtTrig5N)	16	41
IO16P(ExtClk5P)	IO17P(ExtOut5P)	17	42
IO16N(ExtClk5N)	IO17N(ExtOut5N)	18	43
IO18P(ExtTrig6P)	IO19P(ExtClk6P)	19	44
IO18N(ExtTrig6N)	IO19N(ExtClk6N)	20	45
IO20P(ExtOut6P)	IO21P(ExtTrig7P)	21	46
IO20N(ExtOut6N)	IO21N(ExtTrig7N)	22	47
IO22P(ExtClk7P)	IO23P(ExtOut7P)	23	48
IO22N(ExtClk7N)	IO23N(ExtOut7N)	24	49
IO_GND	IO_GND	25	50

NOTE: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

FIGURE 16 IP-BISERIAL-VI-CTRB IO CONNECTOR PINOUT

IO_GND = AC / DC / Open based on J1 header shunt setting.

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions were chosen with noise immunity and cable compatibility in mind. The pairs should be connected with twisted pair wiring compatible with a 100 ohm system for best results.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the 485/LVDS devices rated voltages.

If induced noise is causing errors, please check the cabling and make sure the shields are properly tied to ground on one side. It may be necessary to go to higher grade cable. Please note that the shield ground on the card is connected to a header to allow user programming to a DC ground, AC [.1uF cap to ground] or open.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-BiSerial-VI-CTRB is constructed out of 0.062 inch thick high temp ROHS compliant FR4 material.

Options are available for ROHS and standard processing of the SRAM based versions with either connector type. The FRAM option is only available with ROHS processing.

Through hole and surface mounting of components are used.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of .89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if .89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-BiSerial-VI-CTRB design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Host Interface:	IP Module 8 and 32 MHz capable
IO Interface:	8x 3 differential pairs [Trigger, Clock, Pulse]
Tx Data rates generated:	Internal clock rate is 1 MHz, External clocks are independent. Boards are tested with 1 MHz external reference. Timing indicates higher rates will work.
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers [except vector] to 0.
Access Modes:	IO, Memory, ID, INT spaces (see memory map)
Wait States:	minimized based on programmed clock rate
Interrupt:	Programmable per channel/mode
Onboard Options:	Most Options are Software Programmable. Shunt for IO ground reference: open, DC, AC
Interface Options:	24 differential pairs plus reference on P2.
Dimensions:	Type II
Construction:	High temp ROHS compatible FR4 Multi-Layer Printed Circuit, Through Hole and SMT.
Temperature Coefficient:	.89 W/^{o}C for uniform heat across IP
Power:	Typical **180** mA @ 5V typical.
Temperature Range	–40C⇔85C or better rated components. Conformal Coating option for condensing environments

Order Information

IP-BiSerial-VI-CTRB	IP Module with Counter Timer and One Shot capability. 8 ports each with Clock in, Trigger In, and Pulse Out. Internal clock reference is 1 MHz – 1 uS pulse granularity. 32 bit counter to defined One Shot pulse width out, and delay to output a 1 uS pulse in the Counter modes.
-CC	Conformal Coating option
-ROHS	Change to ROHS processing. Without this option, standard leaded solder will be used.
-LVDS	RS-485 is standard for this design. To receive with LVDS IO add this option.
Eng Kit–IP-BiSerial-VI-CTRB	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender IP-BiSerial-VI-CTRB Driver and reference software Technical Documentation, 1. IP-BiSerial-VI-CTRB Schematic Data sheet reprints are available from the manufacturer's web site reference software.

Note: The Engineering Kit is strongly recommended for first time purchases.

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not guaranteed to be current or complete manufacturing data, nor is it part of the product specification.